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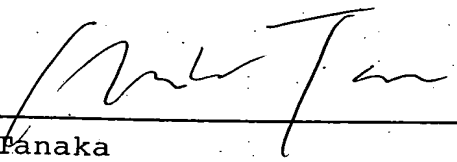
Translator's signature: 

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Specification

Driving Circuit, Driving Method, and Defect Inspection Method for Liquid Crystal Display Devices, and A Liquid Crystal Display Device

Claims

1. A driving circuit of liquid crystal display devices having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:
said driving circuit is characterized in that two or more stages of a shift register of electrically successive multiple stages within said timing control circuits output same output signals at the same timing.

2. A driving circuit of liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:
said driving circuit is characterized in that an output terminal of said shift register of electrically successive multiple stages within said timing control circuits is connected to said sampling circuit or said latch circuit by means of a gate circuit, level shift circuits and so on, or that an output terminal of said shift register of electrically successive multiple stages is connected directly to said sampling circuit or said latch circuit, and that successive M circuits of said M x N sampling circuits and latch circuits are connected to the same video signal line.

3. A driving circuit of liquid crystal display devices having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:
said driving circuit is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that two or more stages of a shift register of electrically successive multiple stages within said timing control circuits output same output signals at the same timing.

4. A driving circuit of liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:
said driving circuit is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, sampling or latch is performed at the timing of an output of said gate circuit, and that successive M circuits of said M x N sampling circuits and latch circuits are connected to the same video signal line.
5. In any of Claims 1 to 4, a driving circuit of liquid crystal display devices characterized by being constructed by thin film transistors (TFTs) which are formed simultaneously with pixel area on the same glass substrate.
6. In a driving circuit of liquid crystal display devices having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:
the driving method of liquid crystal display devices is characterized in that two or more stages of a shift register of electrically successive multiple stages within said timing control circuits output same output signals at the same timing.
7. In a driving circuit of liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:
the driving method of liquid crystal display devices is characterized in that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is 1/N or 1/2N of that of video signals before they are positioned in parallel and that a single start pulse is input in 1H.
8. In a driving circuit of liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving method of liquid crystal display devices is characterized in that an output terminal of said shift register of electrically successive multiple stages within said timing control circuits is connected to said sampling circuit or said latch circuit by means of a gate circuit, level shift circuits and so on, or that an output terminal of said shift register of electrically successive multiple stages is connected directly to said sampling circuit or said latch circuit, and that successive M circuits of said M x N sampling circuits and latch circuits are connected to the same video signal line, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is 1/N or 1/2N of that of video signals before they are positioned in parallel and that a single start pulse is input in 1H.

9. In a driving circuit of liquid crystal display devices having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving method of liquid crystal display devices is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that two or more stages of a shift register of electrically successive multiple stages within said timing control circuits output same output signals at the same timing, and that a clock signal and said enable signal are interrupted during blanking period when video signals are not input.

10. In a driving circuit of liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving method of liquid crystal display devices is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is 1/N or 1/2N of that of video signals before they are positioned in parallel and that a single start pulse is input in 1H, and that a clock signal and said enable signal are interrupted during blanking period when video signals are not input.

11. In a driving circuit of liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving

said sampling circuit and said latch circuit, wherein:

the driving method of liquid crystal display devices is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that successive M circuits of said M x N sampling circuits and latch circuits are connected to the same video signal line, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is 1/N or 1/2N of that of video signals before they are positioned in parallel and that a single start pulse is input in 1H, and that a clock signal and said enable signal are interrupted during blanking period when video signals are not input.

12. In any of Claims 6 to 11, a driving method for a driving circuit of liquid crystal display devices characterized by being constructed by thin film transistors (TFTs) which are formed simultaneously with pixel area on the same glass substrate.

13. A liquid crystal display device having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the liquid crystal display device is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that two or more stages of a shift register of electrically successive multiple stages within said timing control circuits output same output signals at the same timing, and that a clock signal and said enable signal are interrupted during blanking period when video signals are not input.

14. A liquid crystal display device having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the liquid crystal display device is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is 1/N or 1/2N of that of video signals before they are positioned in parallel and that a single start pulse is input in 1H, and that a clock signal and said enable signal are interrupted during blanking period when video signals are not input.

15. A liquid crystal display device having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample

said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the liquid crystal display device is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that successive M circuits of said M x N sampling circuits and latch circuits are connected to the same video signal line, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is 1/N or 1/2N of that of video signals before they are positioned in parallel and that a single start pulse is input in 1H, and that a clock signal and said enable signal are interrupted during blanking period when video signals are not input.

16. In any of Claims 13 to 15, a liquid crystal display device characterized by being constructed by thin film transistors (TFTs) which are formed simultaneously with pixel area on the same glass substrate.

17. In an inspection method for liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines, and a timing control circuit which controls the timing for driving said sampling circuit, wherein:

the inspection method is characterized in that an output terminal of said shift register of electrically successive multiple stages within said timing control circuits is connected to said sampling circuit by means of a gate circuit, level shift circuits and so on, or that an output terminal of said shift register of electrically successive multiple stages is connected directly to said sampling circuit, and that successive M circuits of said M x N sampling circuits are connected to the same video signal line, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is 1/N or 1/2N of that of video signals before they are positioned in parallel and that a single start pulse is input in 1H when signals are input in data lines, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is set at random and that a single start pulse is input in a period 3 times as long as 1H, and that therefore data lines are selected sequentially to perform an inspection.

18. In Claim 17, an inspection method for liquid crystal display devices characterized by being constructed by thin film transistors (TFTs) which are formed simultaneously with pixel area on the same glass substrate.

19. In an inspection method for liquid crystal display devices having sampling circuits which sample video signals and writes them in data lines, and a timing control circuit which controls the timing for driving said sampling circuit, wherein:

the inspection method for liquid crystal display devices is characterized in that any single sampling circuit is set in state of low resistance by interrupting clock signals of shift register within said timing control circuits, and that an inspection is performed during the interruption period.

20. In Claim 19, an inspection method for liquid crystal display devices characterized by being constructed by thin film transistors (TFTs) which are formed simultaneously with pixel area on the same glass substrate.

21. A driving circuit of liquid crystal display devices having video signal lines wherein analog video signals or digital video signals are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving circuit of liquid crystal display devices is characterized in that an output of the shift register within said timing control circuits is input to XOR gate and that a sampling circuit or a latch circuit is driven at the timing of output signals of said XOR gate.

22. In Claim 21, a driving circuit of liquid crystal display devices characterized by being constructed by thin film transistors (TFTs) which are formed simultaneously with pixel area on the same glass substrate.

23. A driving circuit of liquid crystal display devices having video signal lines wherein analog video signals or digital video signals are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving method of liquid crystal display devices is characterized in that an output of the shift register within said timing control circuits is input to XOR gate and that a sampling circuit or a latch circuit is driven at the timing of output signals of said XOR gate, and that a start pulse of said shift register is a square wave at a period of 2 horizontal scan periods (2H).

24. In Claim 23, a driving method for liquid crystal display devices characterized by being constructed by thin film transistors (TFTs) which are formed simultaneously with pixel area on the same glass substrate.

25. A driving circuit of liquid crystal display devices having video signal lines wherein analog video signals or digital video signals are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the liquid crystal display devices is characterized in that an output of the shift register within said timing control circuits is input to XOR gate and that a sampling circuit or a latch circuit is driven at the timing of output signals of said XOR gate, and that a start pulse of said shift register is a square wave at a period of 2 horizontal scan periods (2H).

26. In Claim 25, a liquid crystal display device characterized by being constructed by thin film transistors (TFTs) which are formed simultaneously with pixel area on the same glass substrate.

27. In a driving circuit of liquid crystal display devices having data line driving circuits on the both

side of data lines, wherein:
the driving circuit of liquid crystal display devices is characterized in that one of said data line driving circuits is line sequential which writes digital video signals in data lines and another one of the other side is point sequential which writes analog video signals in data lines.
28. In a driving circuit of liquid crystal display devices having data line driving circuits on the both side of data lines, wherein:
the inspection method for liquid crystal display devices is characterized in that one of said data line driving circuits is line sequential which writes digital video signals in data lines and another one of the other side is point sequential which writes analog video signals in data lines, and that defect inspection is performed in the manner in which data lines are driven by said line sequential data line driving circuit and selected sequentially by said point sequential data line driving circuit.
29. In Claim 27 or Claim 28, a driving and inspection method for liquid crystal display devices characterized by being constructed by thin film transistors (TFTs) which are formed simultaneously with pixel area on the same glass substrate.
30. In a driving circuit of liquid crystal display devices having data line driving circuits on the both side of data lines, wherein:
the liquid crystal display device is characterized in that one of said data line driving circuits is line sequential which writes digital video signals in data lines and another one of the other side is point sequential which writes analog video signals in data lines.

Description of the Invention

Field of Technology

This invention pertains to a liquid crystal display device, a driving circuit and its driving methods for liquid crystal display devices in which thin film transistors are used, and defect inspection methods.

Prior Arts

In a liquid crystal display device which displays image data using electrooptical characteristics of a liquid crystal, excellent display quality is achieved successfully by forming thin film elements such as thin film transistors (TFTs) on a transparent substrate as switching elements of each pixel, and by controlling voltage to be applied on the liquid crystal. Further, an integration technology of driving circuit in which a driving circuit of liquid crystal displays is formed from TFTs in a periphery of an active matrix as one on a substrate instead of using a LSI is now widely used. The integration technology of driving circuit enabled a reduction in size and cost of liquid crystal display devices. Recently an integration technology of driving circuit constructed with TFTs for liquid crystal display devices of 5 to 10 inch class using low temperature process is studied commonly.
Generally, in an active matrix type liquid crystal display device, a pixel matrix 22, a scan line driving circuit 21, and a data line driving circuit 12 are formed on the face of a transparent substrate

11, as shown in a block chart of Figure 1. Figure 1 especially indicates the case in which the driving circuit of liquid crystal display devices which displays analog video signals are integrated using TFTs. A scan line driving circuit 21 has a scan line driving timing control region and a buffer circuit, and output signals of the buffer circuit drive scan lines Y1, Y2, Y3, and so forth. When the scan line is in the selected state, a pixel TFTs 4 connected to it shows low resistance, then the state in which video signals can be written in liquid crystal capacitance 2 and retention capacitance 3 is achieved. The data line driving circuit has a shift register, a timing control circuit made of a gate circuit and so on, switch circuits SW1, SW2, SW3 and so forth constructed with TFTs, and video signal lines V1, V2, and V3. In each of switch circuits SW1, SW2, SW3 ... (from side of the timing control circuit), switch circuit driving signals output from the timing control circuit is ready to input by means of switch circuit driving gate lines G1, G2, G3, and so forth. Therefore, when the switch circuit driving signals are input to each switch circuit SW1, SW2, SW3... by means of the switch circuit driving gate lines G1, G2, G3..., each switch circuit SW1, SW2, SW3...is switched from the state of high resistance to low resistance. Through this switching process, the video signals supplied to the video signal lines V1, V2, and V3 are held by data lines X1, X2, X3 ..., meanwhile at pixels P1, P2, P3 ..., the video signals display the screen changing the orientation state of liquid crystal in a liquid crystal cell 2. In a driving circuit which displays analog video signals, a shift register in a data line driving circuit needs to have enough speed for sampling video signals.

A circuit configuration of shift register is shown in Figure 3. Here, a single stage of the shift register is a single unit of repeated shift register circuit pattern, and a single output signal is output in a single stage. In Figure 3, a region marked with dotted lines is regarded as a single stage, and therefore 3 stages are shown. The signals which are input to the shift register are clock signals CL1, CL1* which determine the operation speed of the shift register, and a start pulse SP, which show a waveform shown in a timing chart of Figure 5. On the other hand, output signals for each of the point a, b, c in Figure 3 corresponds to the points a, b, c of the timing chart of Figure 5. Sometimes the signals of the point a, b, c drive the switch circuit, however, generally timing is controlled inputting the output signals of the shift register to a NAND gate or a NOR gate, not to damage the resolution. Figure 4 shows a NAND gate (left) and a NOR gate (right). If, for example, output of the shift register a, b and b, c of Figure 3 are 2 input of a NAND gate and d and e are its output terminals respectively, signals of each output terminals a to e of shift register and NAND gate are as shown in Figure 5. In this manner, better resolution is realized because there is no overlap between driving timing of adjacent switch circuits. As shown in the timing chart of Figure 5, when the shift register of Figure 3 is used, possible sampling frequency is twice as high as clock frequency which drives the shift register.

Figure 2 illustrates the configuration of a liquid crystal display device having data line driving circuits which display digital video signals. The output signals of the shift register control the timing through gate circuits and so on, then in this output timing digital video signals are latched by latch A. Using this method data are entered in latch A and therefore latch A may be called register. When

data for a single line are latched, they are transmitted to latch B, then video signals D-A converted through D-A converter based on the data are written in the data lines. What requires the fastest speed in the data line driving circuit is a circuit which latches the digital video signals for a single line sequentially, and it need to be fast enough to drive the shift register. In short, the speed to take in the video signals depends in the speed of shift register irrespective of which of analog / digital video signals are displayed.

Forming a driving circuit simultaneously with a pixel region on an insulated substrate using TFTs enables high added value and cost reduction as mentioned above. However, on the other hand, the circuits constructed from TFTs have a shortcoming that it cannot perform at high speed as circuits constructed from transistors on single crystal silicon can do. This is because TFTs are inferior to the transistors on single crystal silicon in electrical characteristics. Especially in the data line driving circuit which requires high speed data write-in, the circuit constructed from TFTs just as it is cannot provide enough speed. For example, the frequency in which VGA video signals are sampled is about 30MHz, and for High-Vision video signals, it is as high as 100MHz and more. On the contrary, the limit of performance speed for a shift register constructed from TFTs of high temperature process is about 20MHz even when the power voltage is 15v. Further, the performance speed is lowered to from 1/5 to 1/10 when TFTs formed through low temperature process are used.

The following are 3 conventional technologies to sample high speed signals using low speed TFTs circuits.

The first technology is the method in Japanese Unexamined Patent Application Showa 60-52892 in which shift registers are set in series. This is a method of increasing substantial sampling frequency by using output of multiple series of shift registers driven by clock signals of different phases as sampling signals. Figure 6 gives an outline of the driving circuit. V and AS indicate video signal line and analog switch, respectively. When sampling signals are input to analog switch, analog switch samples video signals from the video signal line then writes them in data lines. The signals which drives the analog switch are generated by a shift register in a timing control circuit. In some cases the analog switch is driven in the timing of the output signals of the shift register, but in many cases the pulse width of the sampling signals is controlled by means of a gate circuit. In Figure 6, there are 4 series of shift registers and these are driven by clock signals CL1, CL2, CL3, CL4 with phases shifted by pi/4 each. Since the analog switch is driven sequentially by the output signals of these 4 series of shift registers, the first, 5th, 9th, ... analog switches of SR1 in Figure 6 are driven for example. As stated above, the shift register in Figure 3 inherently has the sampling frequency which is twice as high as the clock frequency and therefore the sampling frequency 8 times as high as the clock frequency can be obtained by allocating the analog switches which drive as shown in this example to 4 series of shift registers. Taken from the other way, it is possible to reduce the time of performance for each of the shift registers to one eighth of the sampling frequency.

The second technology is a method in which the data line driving circuits are divided into multiple blocks as disclosed in Japanese Unexamined Patent Application Showa 61-32093. In this method,

first the data line driving circuits are divided into multiple blocks then video signals set in parallel is input to each block to drive the driving circuits of each block simultaneously. The clock frequency of the shift register in a single block is reduced by this method. Figure 7 shows an outline when the driving circuits are divided into 4. V1a to V1d indicate video signal lines, in each of which video signals set in parallel are input. Figure 9 schematically illustrates how the video signals are set in parallel. When the driving circuit of Figure 6 is used, for example, the video signals themselves do not have to be touched and therefore the video signals for a single line is lined up successively. On the other hand, data must be rearranged before they are set in parallel as shown in Figure 9(2) when the driving circuits in a block in Figure 7 are used. In Figure 7 AS indicates analog switches. All the analog switches in a single block are connected to the same video signal line. A common signal is input to each of the blocks as a start pulse of the shift register, therefore, the shift registers of each block starts simultaneously. For example, as shown in Figure 9, when there are 16 pixels in a single line, the video signals are written in the first, 5th, 9th, 13th data lines because all the blocks drives at the same time if the data line driving circuits are divided into blocks. In this manner, the driving frequency of each shift register can be reduced to one eighth.

As the third technology, a collective drive of analog switches is described from page 609 of the SID Digest (1992) and so on. This is a driving method in which multiple analog switches are driven collectively by a single output of a timing control circuit and the video signal is written in the data lines in parallel by the analog switches. Figure 8 shows an example of the driving circuit. The shift register is driven by a series of the clock signals, and the multiple analog switches are driven by sampling signals whose timing is controlled in a gate circuit. In Figure 8, for example, since 4 analog switches perform sampling simultaneously, the frequency of the sampling signal needs to be only one forth of the sampling frequency, and as a result, a driving frequency of the shift register can be reduced to one eighth of the sampling frequency. In this case, the video signals set in parallel are input to the video signal lines, which is schematically shown in Figure 9(3).

As mentioned above, there are 3 conventional methods for reducing the driving frequency of the shift register, which are : setting shift registers in series, dividing the data line driving circuits into multiple blocks, and a collective drive of analog switches. Although only the case in which the analog video signals are sampled is described so far, the same idea can be applied to the circuits which latches digital data. The above technologies are applicable as methods for reducing the driving frequency of the shift register without affecting the speed of latch signals which latch the video signals to a latch circuit.

In a driving circuit of liquid crystal display devices, the timing for driving neighboring sampling circuits is set so that there are no overlaps, by inputting output signals of the shift register to the gate circuit, as shown in Figure 1. However, it is difficult to keep the output pulse width regular when NAND gate or NOR gate is used as a gate circuit, due to the difference in characteristics of P-channel and N-channel transistor. To keep away from this problem, a conventional method in which overlapping is prevented between neighboring analog switches is adopted as described from

page 55 of the SID Digest (1992). In this technology, a driving signal of Nth analog switch is used as a single input of NAND gate which determines the timing for driving of (N+1)th analog switch, and by this (N+1)th analog switch is turned on after Nth analog switch is confirmed to be turned off. Beside, recently the technology striving for reduced power consumption is taken on greater importance as a property required for liquid crystal display devices. The power consumed in the shift register depends on the probability for the signals of the shift register to transit within a unit time and the voltage of the signals. Figure 18 shows a circuit configuration of the timing control circuit which includes a conventional shift register and a timing chart of the internal signals. For example, when 1H is regarded as a unit of time, power voltage reduction is the only way to realize reduced power consumption because the transition probability is the same if the frequency of the clock signal is the same. Further, the transition probability cannot be changed within the shift register, for example at the points of a, b, c, so long as the current driving method is used. So far a method in which the driving voltage of the driving circuit is lowered has been applied to strive for reduced power consumption, because that is the quickest way. Therefore, as matters stand now, the realization of reduced power consumption by means of improving the driving circuit itself is not undertaken yet.

There are 2 broad types of data line driving circuits. One is a point sequential data line driving circuit, and the other is a line sequential data line driving circuit. A point sequential data line driving circuit successively writes the video signals in every data lines as is explained herein above. On the other hand, a line sequential data line driving circuit first retains the video signals for a single line and then writes them in all the data lines taking a time of 1H, like driving circuits which write digital data. Generally the line sequential data line driving circuit is made of IC and assembled in the periphery of a glass substrate which has a pixel region formed from TFTs or the like. Accordingly, to perform an inspection for a driver, all the IC need to be inspected before they are assembled. On the other hand, so far no insoection method is suggested for the case in which the line sequential data line driving circuit is integrated in the periphery of the pixel region using TFTs.

Problems to Be Solved by the Invention

There are 3 broad methods of reducing the driving frequency of the shift register, which will be explained herein below.

In the method in which the shift registers are set in series, clock signals with phases shifted by pai/4 for each series of the shift registers need to be generated then input to the shift registers. In order to drive 4 series of the shift registers, for example, 8 phases of the clock signals are necessary including the clock signals of opposite phases. This leads to an increase of the terminal and of the load on external circuits when, for example, the driving circuit is formed on the glass substrate using TFTs and is driven by the signals generated in the external circuit.

Next, in the method in which the shift registers are divided into multiple blocks, only a single series of the clock signals are necessary, and a line memory to rearrange data for a single line is enough.

However, since the start pulses are input to each block, as shown in Figure 7, the wiring for the start pulses need to reach throughout each of the blocks. Therefore, at least spaces for the wiring are necessary between the blocks, which is a problem in small panels of high precision which requires precise layouts. Further, it was found that the start pulses are affected by noise due to the complicated wiring, and that it causes the changes of output signals of the shift registers on the boundary of the blocks. Hence, this leads to a problem that the boundary of the blocks are displayed non-successively.

Last, in the method in which multiple analog switches or latch circuits are driven collectively, the load increases because multiple neighboring switches or circuits are driven simultaneously, resulting in longer delay time within the circuits. For example, if 4 analog switches or 4 latch circuits are to driven, the capacity of 4 times as large as that of the case in which one switch or circuit is driven is required. Accordingly buffer circuits are required, for example, in which a delay time is arisen, causing a shift in the timing of writing in of the video signals or latching. Further, in the event of inspection, it takes a long time to detect the position of the defect resulting in a bad inspection efficiency, because multiple switch circuits or latch circuits are driven at the same time.

In the conventional technology in which the overlapping of the driving timing of analog switches is prevented, the driving signals themselves of the neighboring analog switches are used as feed forwards. However, NAND gates are used in this case, too, which do not solve the fundamental problem of difference between the width of the output pulses and the original pulses which always appears when there is a difference in characteristics of P-channel and N-channel transistors. Therefore, allowable dispersion of the characteristics which is required for the transistors to keep the resolution of the video display constant is so small that the yield is lowered as a result.

On the other hand, reducing the power voltage is the only measure taken to lower power consumption.

When the line sequential data line driving circuit is assembled using ICs, only the circuits for inspection need to be formed in addition. However, when the line sequential data line driving circuit is integrated on the glass substrate using TFTs, it is difficult to perform inspection on it. Since the signals are written in all the data lines simultaneously in the line sequential data line driving circuit, it is impossible to identify a data line with the point of breaking down, for example.

In consideration of the above problems, the purpose of this invention is to provide liquid crystal display devices and driving circuits, driving methods, and inspection methods for liquid crystal display devices with high display quality and inspection efficiency, which prevent the number of terminals from increasing while reducing the clock frequency of the data line driving circuit and the load on the external circuits, and can be applied in precise layout. The other purpose is to provide liquid crystal display devices and driving circuits, driving methods for liquid crystal display devices with low power consumption, whose resolution of video display is not affected by the dispersion of transistor characteristics. The further purpose is to provide liquid crystal display devices and driving circuits, inspection methods for liquid crystal display devices with high inspection efficiency,

which can display both digital and analog video signals.

Steps Taken to Solve the Problems

This invention is characterized in that 2 or more stages of the electrically successive multiple stages of shift registers output the same output signals simultaneously in 1H, to reduce the driving frequency of the shift register while solving the above mentioned problems.

This invention is further characterized in that the output of electrically successive M ($M \geq 2$) stages of the shift register in the timing control circuit is input to the XOR gate, at the timing of which analog video signals are sampled or digital video signals are latched, and that the start pulse of the shift register is a square wave at a period of 2H/n (wherein n is any positive integer).

The liquid crystal display devices of this invention have 2 data line driving circuits, one of which also serves as a inspection circuit. This configuration strives for yield improvement and better inspection circuit efficiency.

Examples

(Example 1)

In a driving circuit of liquid crystal display devices of this invention having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

said driving circuit is characterized in that two or more stages of a shift register of electrically successive multiple stages within said timing control circuits output same output signals at the same timing.

Figure 10 shows a configuration of the examples of this invention. The liquid crystal display device of this invention has a scan line driving circuit and a data line driving circuit in the periphery of the pixel region which is formed from TFTs. The scan line driving circuit sequentially selects the scan lines one by one, and the time allocated to an each single scan line is 1H. A pixel TFT whose gate electrode is connected to the scan line in the selected state is set in state of low resistance and therefore the video signals can be written in during the scan signals are applied. For example, in the driving signals of VGA, the selection period in which the scan lines are in the selected state is 4/5 of 1H, and the rest is allocated to the blanking period. Further, generally the period in which the video signals are written in is shorter than the selection period of the scan lines. This is because a margin of time for an electrical potential of the scan line to make the resistance of TFTs low enough is taken into consideration. The data line driving circuit is constructed by the shift register SR of clock signal 1 group, a gate circuit, an analog switch AS connected to the data lines, and video signal lines V1a - V1d. The output of the timing control circuit within the data line driving circuit controls the

timing for driving the analog switch, and video signals are written in the data lines according to the timing. The clock signals CL1 and CL1* having the phase shifted by pai are input to the shift register within the timing control circuit. The performance speed of the shift register depends on the frequency of the clock signals. A start pulse SP is input to the shift register when a scan line fall in the selected state and the timing in which the video signals can be written in has come.

In the driving circuit of this invention, the driving circuit of the shift register within the data line driving circuit, or clock frequency, can be set lower than the conventional frequency. When video signals which are not set in parallel by means of the electrically successive multiple stages of the shift register are to be written in to all the data lines, the clock frequency of the shift register is equal to or half of that of the video signals. (This depends on the structure of the shift register. With the shift register of Figure 3, it would be half.) For example, in order to reduce the driving frequency of the shift register to 1/8 of the sampling frequency, the analog switch is connected to 4 video signal lines, as shown in Figure 10. The video signals of each video signal lines V1a - V1d are set in parallel as shown in Figure 9(2). Here, the case in which the number of the pixels connected to a single scan line is 16 is described as an example. The clock signals input to the shift register are indicated as CL1, CL1* in the timing chart of Figure 11. The start pulse indicated as SP in Figure 11 is input here. Then, the output of each shift register a-e and the output signals f-k of the case when NAND gate is used as a gate circuit are as shown in Figure 11. When the output of the shift register a, b or b, c is input to NAND gate, the output of the NAND gate will be f or g, respectively. As a result, several stages of the electrically successive shift registers of multiple stages output the same output signals at the same timing. In this invention, for example, signals are simultaneously output from 4 of the 16 output terminals of NAND gate in a moment. Hence, the 1(f)th, 5(j)th, 9th, 13th analog switches simultaneously perform sampling, for example. Since these analog switches are connected to different video signal lines where the data set in parallel is respectively input, they sample each video signals and write them in the data lines. In this manner, the clock frequency which drives the shift register can be reduced without changing substantial sampling frequency. If the circuit configuration of this invention is used, a sampling frequency which is 8 times as high as the clock frequency of the shift register is obtained by setting the video signals in parallel in 4 phases, since the shift register inherently has a sampling frequency twice as high as its driving frequency.

In the driving circuit of this invention, only a single series of clock signals is required, and therefore it overcomes a problem in the first conventional technology, that is, it does not give an additional load on external circuits nor increase the number of the terminals of the clock signals. Further, the increase of delay time due to multiple driving of the analog switches is not observed, though it was a problem in a collective drive of analog switches of the third conventional technology. The driving circuit of this invention does not require a complicated wiring layouts of start pulses nor a space between the blocks to input the start pulses, though it is the same as the blocking technology of the second technology in the point that the video signals are written in non-successive multiple data

lines. Thus, it is possible to reduce the clock frequency without using a large space even in small panels of high precision which requires precise layouts.

To be more specific about the circuit configuration of the driving circuit of this invention mentioned above, in a driving circuit of liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

said driving circuit is characterized in that an output terminal of said shift register of electrically successive multiple stages within said timing control circuits is connected to said sampling circuit or said latch circuit by means of a gate circuit, level shift circuits and so on, or that an output terminal of said shift register of electrically successive multiple stages is connected directly to said sampling circuit or said latch circuit, and that successive M circuits of said M x N sampling circuits and latch circuits are connected to the same video signal line. Here, M x N data lines mean the number of the data lines in which the video signals are substantially input, and the data lines used as dummies are not included. Whether the clock frequency is reduced or not depends on into how many phases the video signals are set in parallel. For example, when the video signals are set in parallel in N phases, the video signals for M data lines are input to a single video signal line. Accordingly, M successive analog switches being connected to a single video signal line make it possible that the video signals are written in N data lines simultaneously. Figure 12 shows an example in which video signals set in parallel in 4 phases are written in 40 data lines. Here, M equals 10 because N stands for 4. In other words, 10 analog switches connected to successive data lines are connected to a single video signal line. In Figure 12, 1-15 indicate the driving signals of first - 15th analog switches, and the first - 10th analog switches are connected to a single video signal line. In the driving circuit of this invention, the first, 11th, 21st, 31st analog switches are driven simultaneously as shown in Figures, and these analog switches simultaneously write the video signals set in parallel in the data lines from respectively different video signal lines. After this is performed for a period of 1H, the start pulses which are input to the shift registers are sequentially transferred to drive the 10th sampling circuit last. In the next 1H, the transferred signals drive the 11th - 20th sampling circuits. In this manner, the start pulse which was input first is transferred within the shift register taking a time of 4H.

In a driving circuit of liquid crystal display devices of this invention having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

said driving circuit is characterized in that a gate circuit within said timing control circuits regards

an output of the shift register as an input and enable signals as another input, and that two or more stages of a shift register of electrically successive multiple stages within said timing control circuits output same output signals at the same timing. The driving circuit of this invention uses the shift register of the timing control circuit in Figure 10 and the circuit shown in Figure 13 as a gate circuit. In this Example, the output of the successive shift register is regarded as a single input to the NAND gate within the timing control circuit. An enable signal is used as another input to the NAND gate, and the input terminals of the NAND gate are connected to the enable signal lines E, E* so that they are positioned alternately with the output of neighboring shift register as shown in Figures. The output signals of the shift register and the gate circuit thus can be controlled separately. Figure 11 schematically shows the timing chart of reduction of the clock frequency, however, practically there is a blanking period in a period of 1H, during which no sampling nor latch is performed. Further, actual sampling or latch time is shorter than the selection period of the gate lines. In other words, sampling or latch is performed in a part of the period of 1H, and it is not in the rest of the period. Therefore, in the driving circuit of this invention, sampling and latch circuits need to be interrupted for a certain period of 1H. Hence this invention is characterized in that multiple stages of the shift register output signals of the same timing and that the gate circuit whose input is an enable signal is formed, as mentioned above. Descriptions are discussed below about the fact that the output signals of the shift register and the gate circuit of this invention can be interrupted for a certain period. The timing chart of Figure 13 shows the signals a-h, out1-out4 of each point when the clock signals CL1, CL1*, start pulse SP, enable signals E, E* are input to the driving circuit of this invention. In this case, the phases of the enable signals E, E* are shifted each other by pai, and use the same signals as the clock signal. During the period TS2 in which the clock signal is interrupted, enable signals are basically on a low level. On a moment half a period before the period TS2 is over only an enable signal E drives, then the signal begins to output again from the output out3 of NAND gate again, answering to the drive of E. As it is apparent from this, the output of the shift register and the gate circuit can be interrupted during a period of TS2 in Figures by interrupting the clock signals and the enable signals. Further, after the signal output is interrupted, the shift register and NAND gate can be restarted from the same status as that of before the interruption. In this Example, for example, if the driving circuit is interrupted right after the output of out2 is carried out, the NAND output signal can be restarted from out3, the next output of out2, by restarting the driving circuit after a certain period. In this invention, sampling or latch of the video signals is performed at the desired timing if the period TS2 in Figures is set at the blanking period or the like in which no sampling nor latch is performed, since the output signals of this invention can be interrupted for a predetermined period.

The driving circuit of this invention is characterized in that it can be applied in precise layout. It is therefore particularly effective in the case in which the driving circuit is integrated using TFTs. So far it is still difficult to achieve miniaturization for TFTs formed on a glass substrate, and there is a limit to reduce the size of transistor. Further, the line and space of the wiring itself is in the order of

3-4 μm. Accordingly, a region at least about 10μm is required to set a single start pulse wiring. In small liquid crystal display devices of high precision or the like used for projectors and so on, mainly the pixel pitch is 20μm or below, thus giving a region as large as 10μm to a single start pulse wiring places a large hurdle to miniaturization. This invention is especially advantageous in the point that it can reduce the clock frequency of the shift register achieving the precise layout of TFTs. It is even possible to form a driving circuit using TFTs formed through the low temperature process which is charecterized in that it is difficult to reduce the size and that the transistor characteristics are still poor.

In a driving circuit of liquid crystal display devices of this invention having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving method of liquid crystal display devices is characterized in that two or more stages of a shift register of electrically successive multiple stages within said timing control circuits output same output signals at the same timing. Figure 11 shows the driving method of this invention. The circuit shown in Figure 10 is used as a driving circuit. The clock signals CL1, CL1*, and the start pulse SP are input to the circuit at the timing shown in the Figure. Four stages of the shift register output the signals of the same timing simultaneously by setting the video signals in parallel in 4 phases and thus reducing the driving frequency (clock frequency) of the successive shift registers to 1/4 of that of the case in which the video signals are not set in parallel. The start pulse is successively transferred from the first to the last stage of the shift register by using this driving method. This driving method is the same as that of the blocking technology in the point that in a certain moment the video signals are written in non-successive multiple data lines, however, it does not cause a sudden non-succession in the signals since the start pulse is successively transferred in this driving method. Thus, the problem that the wiring of start pulses are affected by noise causing the changes of output signals of the shift registers and the gate circuits, which is observed in the blocking technology, is solved. Accordingly, uniform write-in is secured without making differences of the write-in characteristics of the video signals to the data lines from a data line to the other. In this manner, the driving method of this invention is characterized in that it reduces the driving frequency of the shift register while keeping the uniformity of the signals.

In a driving circuit of liquid crystal display devices of this invention having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving method of liquid crystal display devices is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that two or more stages of a shift register of electrically successive multiple stages within said timing control circuits output same output signals at the same timing, and that a clock signal and said enable signal are interrupted during blanking period when video signals are not input. In other words, it is characterized in that the same driving as said driving method is performed during the period in which data is sampled, and that the clock signal of the shift register and the enable signals input to the gate circuit are interrupted during the period in which the video signals are not input. It is further characterized in that multiple sampling circuits are always in the selected state simultaneously. Accordingly, all the sampling circuits need to be set in the non-selected state during a period in which the video signals are not input, and they need to be set in the selected state from the moment when the video signals are input again. Therefore, the enable signals are used in the driving method of this invention. These make it possible that the data set in parallel is written in the data lines using the clock signals with reduced frequency and that sampling or latch is interrupted during a period in which the video signals are not input.

To be more specific about the driving method of this invention, in a driving circuit of liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input or N video signal lines wherein digital video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines or M x N latch circuits which latch said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving method of liquid crystal display devices is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that successive M circuits of said M x N sampling circuits and latch circuits are connected to the same video signal line, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is 1/N or 1/2N of that of video signals before they are positioned in parallel and that a single start pulse is input in 1H, and that a clock signal and said enable signal are interrupted during blanking period when video signals are not input. When the configuration shown in Figure 3 is used as a shift register, the clock frequency need to be only 1/2N of that of video signals before they are set in parallel, because the possible substantial output frequency of the shift register is twice as high as the clock frequency, as mentioned above. On the other hand, if the shift register having a output frequency which is equal to the clock signals is used, the clock frequency will be 1/N of that of video signals before they are set in parallel.

Figure 14 shows a driving method of this invention. It shows the case in which the video signals written in 640 data lines are sampled or latched and the video signals are set in parallel in 4 phases. Thus, here N=4, and M=160. The circuit shown in upper portion of Figure 13 is used as the shift

register and gate circuit of the timing control circuit shown in Figure 10. The start pulse, clock signals, and enable signals of lower portion of Figure 13 are input to the circuit in Figure 13. The frequency of the clock signals is 1/4 of the sampling frequency, as mentioned above. The output signals of the gate circuit can be interrupted for a period TS3 including a blanking period in which the video signals are not written in, using the driving method of this invention. Figure 14 shows the output signals of 157th - 162nd stages of the shift register and that of 159th - 164th stages of the gate circuit when the driving method of this invention is used. In Figure 14, GP1 indicates a selection pulse of any scan line and GP2 indicates a selection pulse of the next scan line. 1H indicates 1 horizontal scan period and BL indicates a blanking period. T indicates a portion of 1H in which the video signals are sampled or latched. The video signals are input during the period of T. TS3 indicates the period between the end of sampling or latch in a single line and the beginning of sampling or latch in the next line. In the driving method of this invention, the clock signals and the enable signals are interrupted during the period of TS3, as shown in Figure 14. The timing of the output signal, the signal which determines the write-in timing of the data signals to 159th - 164th data lines, is shown in lower portion of Figure 14 (out159 - out164). As is apparent from the figure, after the 160th video signal is sample or latched, the signals are not output from the gate circuit during the period of TS3, then the video signal of the next line is input and the signal which samples or latches the 161st video signal is output from the gate circuit. In the driving method of this invention, the clock signals and enable signals are interrupted for a period of TS3 and then restarted during the period in which next sampling or latch is performed, as explained above. By this, the sampling and latch can be performed only in a period in which the video signals are input and the reduction of the clock frequency is achieved at the same time. Further, the driving method of this invention can prevent unnecessary waste of power. During the period in which video signals are not input, what consumes the power most in the whole circuits is the portion that performs at high speed. In a driving circuit of liquid crystal display devices, the clock signals and enable signals on the side of the data line driving circuit are the portions. In the driving method of this invention, not only the clock frequency of the shift register can be reduced, but waste of power during a period in which the video signals are not input is prevented, since the clock signals and enable signals are interrupted during this period. Thus the reduced power consumption in driving circuits is achieved.

In a liquid crystal display device having multiple video signal lines wherein analog video signals positioned in parallel in 2 or more phases are input or multiple video signal lines wherein digital video signals positioned in parallel in 2 or more phases are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the liquid crystal display device of this invention is characterized in that a gate circuit within said timing control circuits regards an output of the shift register as an input and enable signals as another input, and that two or more stages of a shift register of electrically successive multiple

stages within said timing control circuits output same output signals at the same timing, and that a clock signal and said enable signal are interrupted during blanking period when video signals are not input. Figure 15 shows a liquid crystal display device of this invention. The liquid crystal display device of this invention is comprised of a liquid crystal display panel which is formed by combining TFT substrate shown in Figure 15 and the counter substrate and then injecting liquid crystal, a back light, external circuits, and so on. The lower portion of Figure 15 shows a circuit configuration on the side of the TFT substrate. The data line driving circuit is made of the circuit configuration shown in Figure 10 and Figure 13, and the driving method shown in Figure 14 is used to display video signals. The liquid crystal display device of this invention provides stable video display without error function, because the clock frequency can be set lower than the sampling frequency. Further, it solves the problem in the conventional technology that vertical lines are displayed in the boundary of the blocks, because the data line driving circuits are not divided into blocks in this invention. It is also characterized in that reduced power consumption is achieved more compared with the conventional liquid crystal display devices, because the data line driving circuit is interrupted during a period in which the video signals are not input.

In a driving circuit of liquid crystal display devices having M x N data lines, N video signal lines wherein analog video signals positioned in parallel in N phases are input, M x N sampling circuits which sample said analog video signals and writes them in data lines, and a timing control circuit which controls the timing for driving said sampling circuit, wherein:

the inspection method for liquid crystal display devices of this invention is characterized in that an output terminal of said shift register of electrically successive multiple stages within said timing control circuits is connected to said sampling circuit by means of a gate circuit, level shift circuits and so on, or that an output terminal of said shift register of electrically successive multiple stages is connected directly to said sampling circuit, and that successive M circuits of said M x N sampling circuits are connected to the same video signal line, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is 1/N or 1/2N of that of video signals before they are positioned in parallel and that a single start pulse is input in 1H when signals are input in data lines, and that a clock frequency which drives a shift register of electrically successive multiple stages within said timing control circuits is set at random and that a single start pulse is input in a period 3 times as long as 1H, and that therefore data lines are selected sequentially to perform an inspection.

Figure 16 shows an Example of the inspection method for liquid crystal display devices of this invention. It schematically shows the case in which the video signals are set in parallel in 4 phases and 640 analog switches are driven, as is the same as the above-mentioned example. The circuit shown in Figure 10 whose data line driving circuit is the circuit of upper portion in Figure 13 is used as a driving circuit. In Figure 16, the numbers 1, 2, 3, ... indicates the first, second, third analog switches respectively. The Os in the figure indicates the periods in which the switches are selected. The table on the upper portion of Figure 16 illustrates the case in which the video signals are

sampled. When the driving method of this invention is used, 4 analog switched are driven simultaneously in a certain moment, as discussed above. The figure illustrates that the first, 161st, 321st, 481st analog switches are first driven simultaneously, and that then the second, 162nd, 322nd, 482nd ones are next driven. In the driving method of this invention, multiple sampling circuits are driven simultaneously as shown in upper portion of Figure 16 when the driving circuit samples the video signals, as mentioned above. On the other hand, it is characterized in that only a single sampling circuit drives as shown in lower table of Figure 16 when inspection is performed. For example, when the video signals are set in parallel in 4 phases like those in Figure 16, 1H is set 4 times longer at the inspection and only a single start pulse is input in this period, if the clock frequency is not changed. Thus, the 640 gate circuits drive sequentially in this period of 4H, and only a single circuit is driven at a time. As a result, for example, when inspection for breaks on data lines is performed by setting a conventional inspection circuit on the both side of the data lines, the location of defects can be quickly detected because the data lines are sequentially selected one by one. For detection of the location of defects, the method in which the data lines are driven sequentially is more effective, offering easy way to identify the location of defects. In the blocking technology or the collective drive of the multiple analog switches of the second and third conventional technology, multiple data lines are always driven and therefore it takes longer to detect the block which has defective signals when these are detected or to detect the data line which contains a defect from all the data lines which are driven collectively. On the other hand, in the driving circuit of this invention, it is characterized in that 2 or more stages of successive multiple stages of shift register output the same output signal at the same timing and drive multiple data lines simultaneously when a panel is driven, and that an inspection is effectively performed by writing the video signals only in a single data line at a time at the defect inspection.

This inspection method is effective especially when the driving circuit of this invention is constructed using TFTs formed on a glass substrate. For liquid crystal display devices with driving circuit ICs added to a substrate on which a pixel region to display image data is only formed, special equipment such as a prover with many pointers is required to perform a defect inspection at the time when the pixel region is completed. On the other hand, when the pixel region and the driving circuit formed using TFTs are simultaneously composed on a single substrate, the additional inspection circuits are not required and instead the integrated driving circuit can be used. Further, the driving method and inspection method of this invention is effective compared with the conventional method in which the driving circuit of TFTs and the pixel region is formed simultaneously on the substrate. The driving method and inspection method of this invention is characterized in that the inspection efficiency is improved by changing the start pulse only when the inspection is performed. This is a special effect which can be obtained by using the driving circuit of this invention as a circuit formed from TFTs on a single glass substrate.

In a driving circuit of liquid crystal display devices having sampling circuits which sample video signals and writes them in data lines, and a timing control circuit which controls the timing for

driving said sampling circuit, wherein:

the inspection method for liquid crystal display devices is characterized in that any single sampling circuit is set in state of low resistance by interrupting clock signals of shift register within said timing control circuits, and that an inspection is performed during the interruption period.

Figures 17, 18 show an Example of the driving method and inspection method of the liquid crystal display devices of this invention. There is a data line driving circuit on one side of the data lines which form a pixel region and an inspection circuit on the other side. The circuit shown in the upper Figure 18 is used for the shift register and gate circuit of the data line driving circuit. The output of the shift register is input to NAND gate, then analog switch is driven by the output of NAND gate. In the inspection circuit, transistors whose source terminals are connected to data lines are connected to the wiring TG which made the gate circuits common, and all the drain terminals are connected to the inspection signal line TC. The timing chart of lower Figure 18 shows the driving method of this invention. The clock signals are interrupted at the moment when the sampling circuit connected to the data line which is to be inspected fall on the selected state. Figure 18 shows the case in which the sampling circuit connected to out3 and the data line connected to the sampling circuit are inspected. Since out2 is always turned on during the period shown in TS1, the analog switch connected to it is also turned on during it is interrupted. Accordingly, a certain data line shown in Figure 17 is connected to the video signal line V1 in the state of low resistance by means of the analog switch. If the voltage which lowers resistance of the inspection transistor is applied to TG, V1 and TC are mutually connected my means of a data line. In this state, the value for electrical characteristics of the data line is obtained by inputting inspection signals from either of V1 or TC and observing a variation of output signals at the other terminal. For example, it is possible to measure the frequency characteristics which shows the limit of write-in of high frequency video signals. This enables to know how much the video signals are written in the data lines at the inspection. Using the driving method and inspection method of this inspection, it is possible to measure the electrical characteristics of a certain analog switch and a data line in a static state.

The driving method and inspection method of this invention is especially effective when the driving circuit using TFTs and the pixel region are formed simultaneously on a glass substrate. When the driving circuit is assembled using ICs or the like, a large-scale prover is required at inspection, on the other hand, there is large flexibility at inspection. However, when the driving circuit is formed on a glass substrate using TFTs, there is a restriction that the driving circuit must be used for the inspection. The driving method of this invention is characterized in that a new inspection is realized only by changing a inspection method for a conventional driving circuit, and it is particularly efficient when the driving circuit is formed on a glass substrate using TFTs.

As the first Example of this invention, the case when analog video signals are written in the data lines by means of the analog switch is explained. The data line driving circuit and driving method of this invention can also be used when the digital video signals are latched by means of the latch circuit. In this case, not only the driving frequency of the shift register is reduced but the above-

mentioned effect is obtained when digital video signals are set in parallel every a bit and written in multiple video signal lines.

(Example 2)

In a driving circuit of liquid crystal display devices having video signal lines wherein analog video signals or digital video signals are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving circuit of liquid crystal display devices is characterized in that an output of the shift register within said timing control circuits is input to XOR gate and that a sampling circuit or a latch circuit is driven at the timing of output signals of said XOR gate.

Figure 20 upper shows an Example of this invention. The shift register is the same as the conventional one, and in this invention its output is input to XOR gate. In an example of the conventional driving method shown in upper part of Figure 19, the output signal of the shift register is input to NAND gate and therefore the timing is controlled. The difference between XOR gates and NAND, NOR gates is found in that NAND, NOR gates determine the output timing depending on setting up and setting off of the output signals, and that XOR gates determine it depending on either of setting up or setting off of the output signals. Now the setting up and setting down of the signals within logic circuits are explained below. In CMOS circuits, P-channel and N-channel transistors are connected to power source Vdd on the side of high voltage and GND, respectively. As an example, inverters are described. When the electrical potential which corresponds to high and the input capacity is charged, the electrical potential of the gate electrode rises to Vdd, which turns on the N-channel transistor then the output capacity is discharged. On the contrary, when the electrical potential which corresponds to low is input and the input capacity is discharged, the electrical potential of the gate electrode falls to GND, which turns on the P-channel transistor then the output capacity is charged. By means of charging/discharging of input/output capacity, the output electrical potential is set off to low by high input or set up to high by low input, and in this manner it works as an inverter. The gate circuit functions similarly. The output signals of the shift register charge/discharge the input capacity of the gate circuit. The case in which, for example, the on resistance of P-channel transistor which constructs the circuit is much higher than that of N-channel transistor, is discussed below. Since the input capacity of the gate circuit is the same, the electrical potential is set off quickly by discharging the capacity, but it sets up only slowly. When this kind of signals are used as input signals of NAND gate or NOR gate, the pulse width of the output signals is not constant as a result. For example, in Figure 19, when b sets up slowly and a sets off quickly, the pulse width of the output signal e is effected by the signal b and therefore it is narrowed. From the other way around, if the characteristics of P-channel and N-channel transistors is exchanged, the output pulse width is extended. On the other hand, when the XOR gate of this invention is used as

shown in Figure 20, the pulse width of the output signal e depends on the setting up of a, b, therefore, the pulse width of the output signal is not extended. Further, the vertical resolution is improved by using the driving circuit of this invention shown in Figure 20 in the data line driving circuit. When the analog switch is driven and the video signals are sampled by the signals which are used for controlling timing, there appear overlaps of driving timing between neighboring pixels if the pulse width of the sampling pulse is extended, thus lowering the resolution because the video signals of neighboring pixels are taken in. The driving circuit of this invention can solve this problem and improve the vertical resolution.

The above driving circuit in which XOR gate is used is especially effective when the circuit is constructed by TFTs. The difference of transistor characteristics between P-channel and N-channel transistors is evident in TFTs formed on an insulated substrate compared with transistors on a single crystal silicon substrate. The dispersion of the transistor characteristics is large even though the TFTs are formed through the same steps. When the TFTs like this is used to form a circuit, the output signals of the driving circuit vary between panels with the conventional driving circuits, because there appears a large gap between the time taken for setting up and setting off. Accordingly, it is very useful especially for the circuit constructed using TFTs to use the XOR gate which can output the signals with constant pulse width without effected by setting up/setting off of the signals as a timing control circuit.

In a driving circuit of liquid crystal display devices having video signal lines wherein analog video signals or digital video signals are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the driving method of liquid crystal display devices of this invention is characterized in that an output of the shift register within said timing control circuits is input to XOR gate and that a sampling circuit or a latch circuit is driven at the timing of output signals of said XOR gate, and that a start pulse of said shift register is a square wave at a period of 2H. As stated in the part about conventional technologies, so far the method in which driving voltage is lowered is applied to reduce the power consumption of the shift register, and a method in which transition possibility of the internal signals is lowered is not studied in the field of shift register constructed using TFTs. However, the driving method of this invention reduces the transition possibility of the signals of the shift register to half of conventional one, thus reducing the power consumption to half. A timing chart in Figure 20 lower shows an Example of the driving method of this invention. CL1 and CL1* indicate clock signals of the shift register and SP indicates a start pulse. These signals are input to the driving circuit in the upper portion of Figure 20. GP indicates a driving signal of any single scan line of a liquid crystal display device. Therefore, GP stays in the state of high for a period of 1H and then turns in the state of low until the next selection period begins. The lower Figure 20 shows the signals of output a-d of the shift register and output e-g of XOR gate when the signals are input to

the shift register to drive it. As is apparent compared with the timing chart of a conventional driving method in lower Figure 19, the transition possibility of signals within the shift register of this invention is evidently reduced to half of that of the conventional driving method, although the same output signals are obtained from the gate circuit. Let us compare the signal b. In the conventional driving method, the signal is set up once and set off once within a period of 1H. In other words, P-channel transistor of a CMOS circuit charges a load capacity once and N-channel transistor discharges the load capacity once. On the other hand, in the driving method of this invention, the signal only sets up once within 1H. Then it sets off within next 1H. Therefore, the same load capacity as the conventional one is charged/discharged within a period of 2H, thus reducing the power consumption to about half.

The driving method of this invention is especially effective when it is used in a driving circuit constructed using TFTs. Since the electrical characteristics of TFTs are worse than that of the transistor formed on a single crystal silicon substrate, it is difficult to drive a CMOS circuit constructed of TFTs with driving voltage of 3.3V or 5V, in which LSIs or the like are driven. Accordingly, the driving voltage of 6-12V is applied usually. Especially for TFTs formed through low temperature process, at least 15V is required as driving voltage. It is necessary to reduce the driving voltage to half to halve power consumption of the shift register, which is almost impossible in the field of current TFTs. Even if it is possible, the reduction of driving voltage narrows the function margin, thus spoiling the reliability of the circuit. Therefore, the driving method of this invention is totally advantageous for the driving circuits using TFTs which require the reduction of power consumption without reducing the driving voltage, because it easily reduces the power consumption to half.

In a driving circuit of liquid crystal display devices having video signal lines wherein analog video signals or digital video signals are input, a sampling circuit which samples said analog video signals and writes them in data lines or a latch circuit which latches said digital video signals, and a timing control circuit which controls the timing for driving said sampling circuit and said latch circuit, wherein:

the liquid crystal display devices of this invention is characterized in that an output of the shift register within said timing control circuits is input to XOR gate and that a sampling circuit or a latch circuit is driven at the timing of output signals of said XOR gate, and that a start pulse of said shift register is a square wave at a period of 2 horizontal scan periods (2H). In liquid crystal display devices of this invention which have the driving circuit shown in Figure 20 within the data line driving circuit, the power consumption of the shift register is reduced to half only by changing the signals of start pulse, without changing any of the driving voltage or driving speed of the shift register in the driving circuit. In other words, the start pulse shown as SP in Figure 19 only have to be changed to the one shown as SP in Figure 20. Since the shift register is used for both of a scan line driving circuit and a data line driving circuit, the whole power consumption of the liquid crystal display device of this invention is much reduced compared with the conventional one. For example,

when it is used in a portable communication device or the like and driven by a battery, it is competent for a long time use.

In the liquid crystal display devices of this invention in which the driving circuit is constructed with TFTs, in particular, the set-up time and set-off time of the scan line driving signals are kept constant even though the TFTs characteristics vary in P-channel and N-channel transistors, and therefore the video signals are written in constantly for a period of 1H and display of good quality without difference between right and left side is obtained. Further, the image of high vertical resolution can be achieved when the driving circuit is integrated on the glass substrate using TFTs, too, because there is no overlap in the driving signals of the analog switch.

(Example 3)

In a driving circuit of liquid crystal display devices having data line driving circuits on the both side of data lines, wherein:

the driving circuit of liquid crystal display devices is characterized in that one of said data line driving circuits is line sequential which writes digital video signals in data lines and another one of the other side is point sequential which writes analog video signals in data lines. Figure 21 shows an Example of a driving circuit of a liquid crystal display device of this invention. The driving circuit of this invention is characterized in that it has 2 data line driving circuits around a pixel region, one of which is a line sequential data line driving circuit and the other is a point sequential data line driving circuit. In Figure 21, the upper data line driving circuit is line sequential and the lower one is point sequential. The line sequential data line driving circuit is composed of a timing control circuit, latch A, latch B, and D-A converter. The timing control circuit is composed of a shift register and a gate circuit, and driven by inputting clock signals CL1, CL1* and a start pulse SP. Digital video signals V1-V4 is taken in by means of latch A. When all the video signals for 1H are taken in, those are transferred to latch B, then converted into analog video signals by D-A converter and written in the data lines. The line sequential driving circuit writes the video signals in all the data lines in 1H, which is often used when digital video signals are displayed. On the other hand, in the point sequential data line driving circuit, the video signals are sequentially written in one data line at a time, which is often used when the analog video signals are displayed. The point sequential data line driving circuit is composed of a shift register, a gate circuit, analog switches AS, and a video signal line V1. In the driving circuit of this invention, the video signals are written in the data lines regardless of whether these are digital or analog, because it has both of the line sequential and point sequential data line driving circuit. If it has only one of them, an additional circuit for converting the analog signals into digital or the way around is required. The driving circuit of this invention can be applied for both kind of signals. Further, in the line sequential data line driving circuit, it is difficult to find out the data line with a point of breaking down at inspection because the video signals are written simultaneously in all the data lines. However, the driving circuit of this invention has a point sequential data line driving circuit which can be used as a inspection circuit on the other side of the

line sequential data line driving circuit. The signals are written in the data lines by means of the line sequential data line driving circuit and the point sequential data line driving circuit performs inspection at the same time. In this manner, the inspection for a point of breaking down in the data lines when the line sequential data line driving circuit is used, which was not easy so far, is now performed in a very effective way.

In a driving circuit of liquid crystal display devices having data line driving circuits on the both side of data lines, wherein:

the inspection method for liquid crystal display devices of this invention is characterized in that one of said data line driving circuits is line sequential which writes digital video signals in data lines and another one of the other side is point sequential which writes analog video signals in data lines, and that defect inspection is performed in the manner in which data lines are driven by said line sequential data line driving circuit and selected sequentially by said point sequential data line driving circuit.

A defect inspection method of this invention is described below. Signals are written in the data lines by means of the line sequential data line driving circuit in the upper portion of Figure 21. At this moment, the signals of the highest voltage, for example, are written in as video signals for all the data lines. Then, the same voltage is written in all the data lines in 1H and the analog switches AS are sequentially driven by means of the point sequential data line driving circuit. The data lines are thus sequentially selected. Now it is possible to detect a point of breaking down when the signal V1 is observed by means of a oscilloscope. If there is no point of breaking down in the data lines, the voltage is observed in all the data lines, and if there is any, the voltage is not observed. Thus, the inspection method of this invention enables the detection of break-down point in the data lines of liquid crystal display devices with the line sequential data line driving circuit.

Effects of the Invention

The purpose of this invention is to provide liquid crystal display devices and driving circuits, driving methods, and inspection methods for liquid crystal display devices with high display quality and inspection efficiency, which prevent the number of terminals from increasing while reducing the clock frequency of the data line driving circuit and the load on the external circuits, and can be applied in precise layout. The other purpose is to provide liquid crystal display devices and driving circuits, driving methods for liquid crystal display devices with low power consumption, whose resolution of video display is not affected by the dispersion of transistor characteristics. The further purpose is to provide liquid crystal display devices and driving circuits, inspection methods for liquid crystal display devices with high inspection efficiency, which can display both digital and analog video signals.

Brief Explanation of the Figures

Figure 1 shows the overall configuration of a liquid crystal display device which displays analog

video signals.

Figure 2 shows the overall configuration of a liquid crystal display device which displays digital video signals.

Figure 3 is a circuit diagram of the shift register shown in Figure 1, 2.

Figure 4 is a circuit diagram which shows an example of the gate circuit shown in Figure 1, 2.

Figure 5 is a timing chart when the shift register of Figure 3 and the gate circuit of Figure 4 are combined.

Figures 6-8 are block diagram which show examples of the circuit configuration of conventional data line driving circuits.

Figure 9 shows how the video signals are set in parallel.

Figure 10 is a block diagram which shows the summary of this invention.

Figure 11 is a timing chart which shows the summary of this invention.

Figures 12-18 show the summary of this invention.

Figure 19 shows the summary of the conventional circuit configuration.

Figures 20, 21 show the summary of this invention.

Explanation of the Symbols

11 ... transparent substrate

12 ... data line driving circuit

21 ... scan line driving circuit

22 ... pixel matrix

V1, V2, V3, V1a, V1b, V1c, V1d ... video signal lines

SW1, SW2, SW3, AS ... switch circuits

P1, P2, P3 ... pixel matrixes

X1, X2, X3, X4, X5, X6 ... data lines

Y1, Y2, Y3 ... scan lines

G1, G2, G3 ... gate lines for driving switch circuits

2 ... liquid crystal cell

3 ... retention capacitance

4 ... pixel transistor

SR, SR1, SR2, SR3, SR4 ... shift registers

CL1, CL1*, CL2, CL2*, CL3, CL3*, CL4, CL4* ... clock signal lines

GP ... scan signal

Summary

Purpose

The purpose of this invention is to achieve the reduced power consumption and yield improvement.

Configuration

In the driving circuit of liquid crystal display devices, the driving circuit and driving method which reduce the driving frequency of the shift register of the driving circuit without changing the sampling frequency of the video signals are provided. Further, the circuit configuration of the data line driving circuit which reduces the power consumption of the shift register to half is provided.

Selected Figure

Figure 10

Name of document: Drawings

Fig. 1

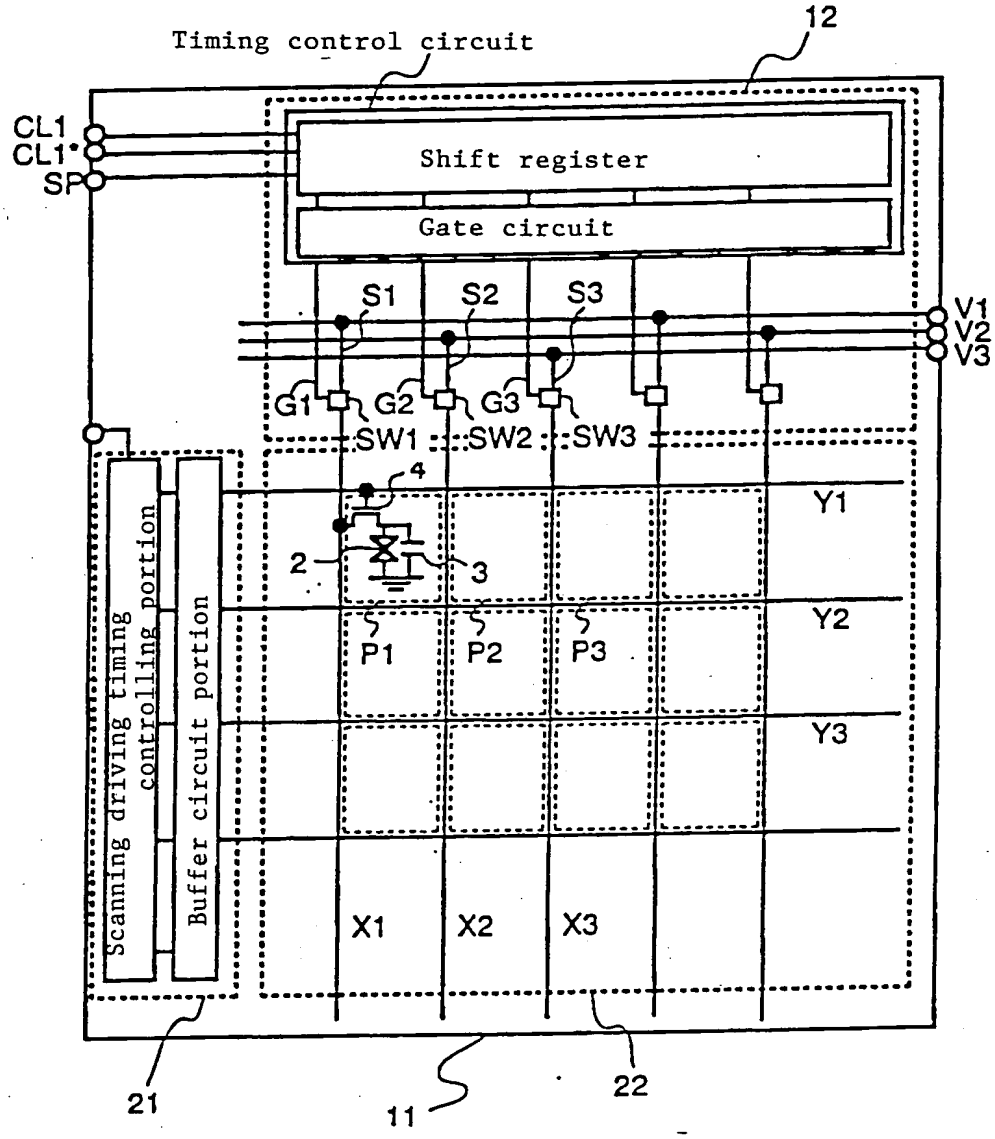


Fig. 2

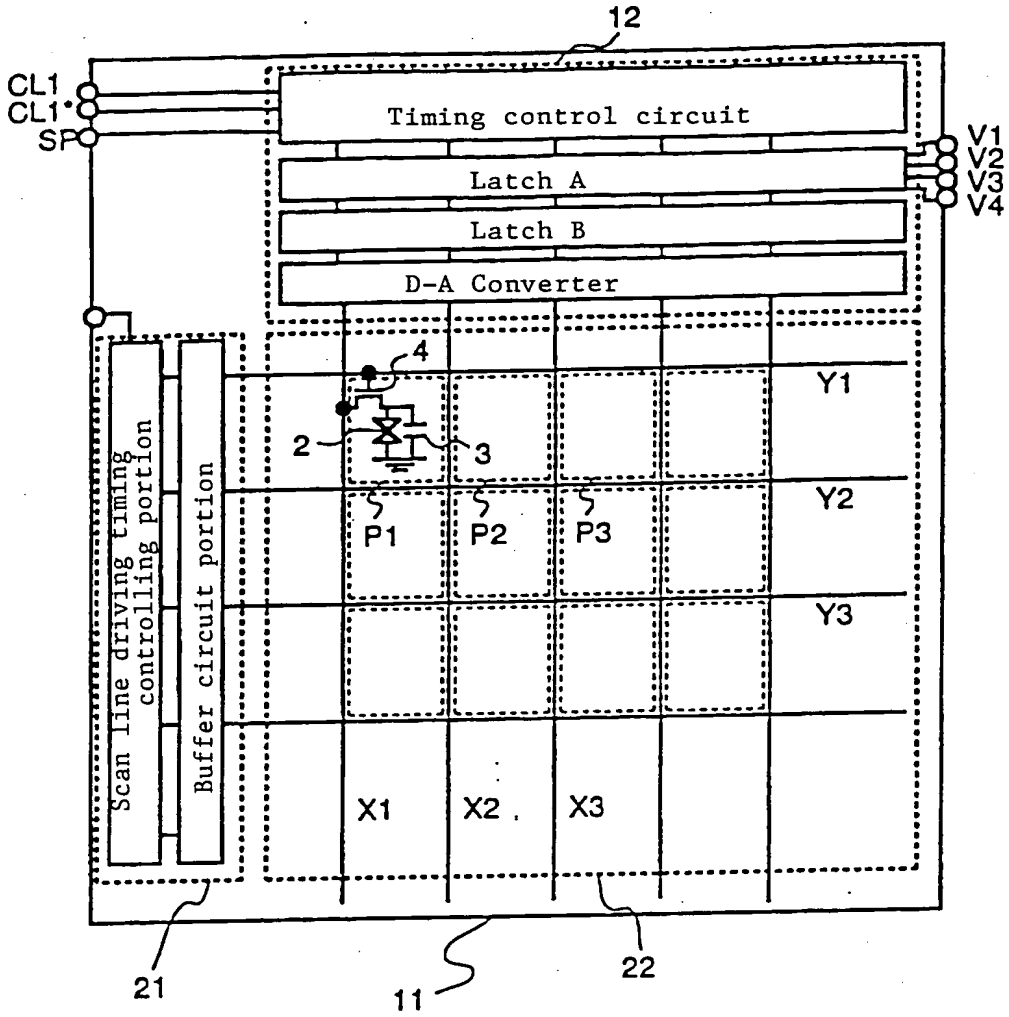

12
CL1
CL1*
SP
Timing control circuit
Latch A
Latch B
D-A Converter
V1
V2
V3
V4
4
2
3
Y1
Y2
Y3
P1
P2
P3
Scan line driving timing controlling portion
Buffer circuit portion
X1
X2
X3
21
11
22

Fig. 3

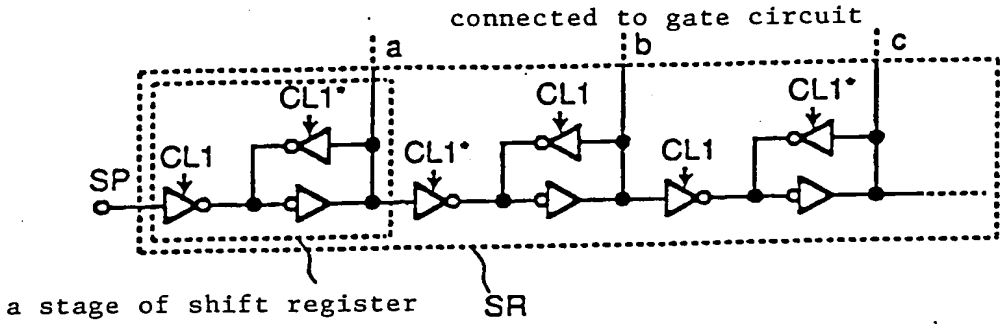

connected to gate circuit
a
b
c
CL1*
CL1
CL1*
CL1
CL1*
CL1
SP
a stage of shift register
SR

Fig. 4

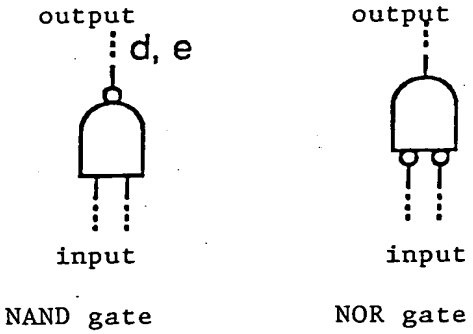

output
d, e
input
NAND gate
output
input
NOR gate

Fig. 5

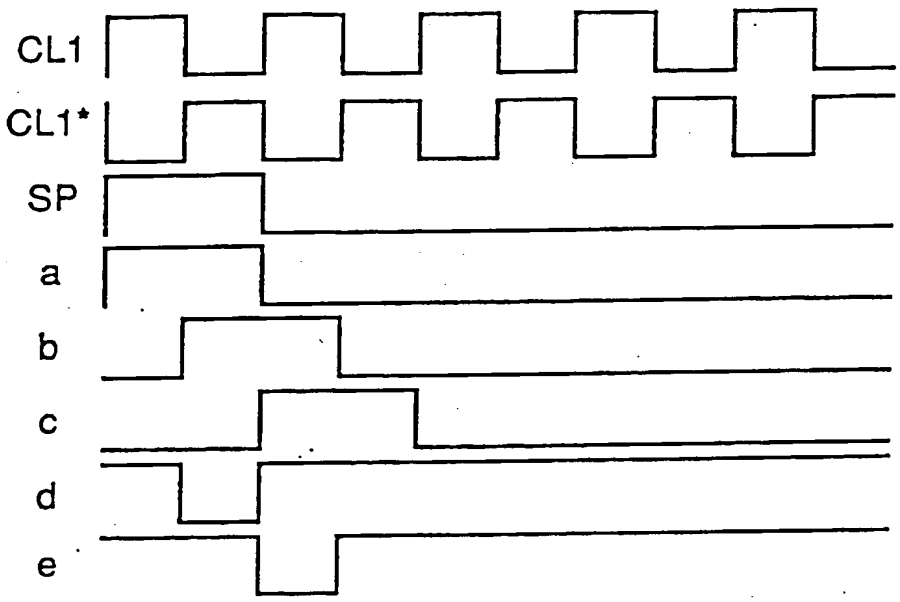


Fig. 6

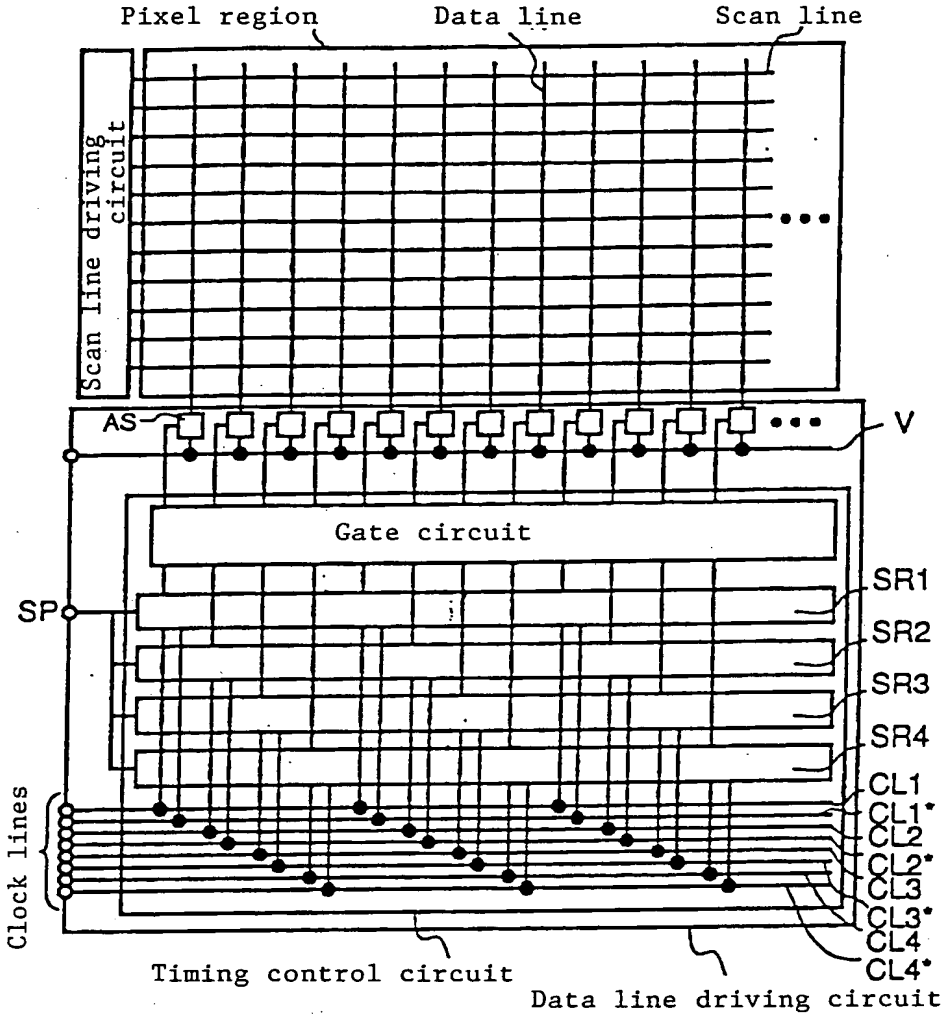

Pixel region
Data line
Scan line
Scan line driving circuit
AS
V
Gate circuit
SP
SR1
SR2
SR3
SR4
Clock lines
CL1
CL1*
CL2
CL2*
CL3
CL3*
CL4
CL4*
Timing control circuit
Data line driving circuit

Fig. 7

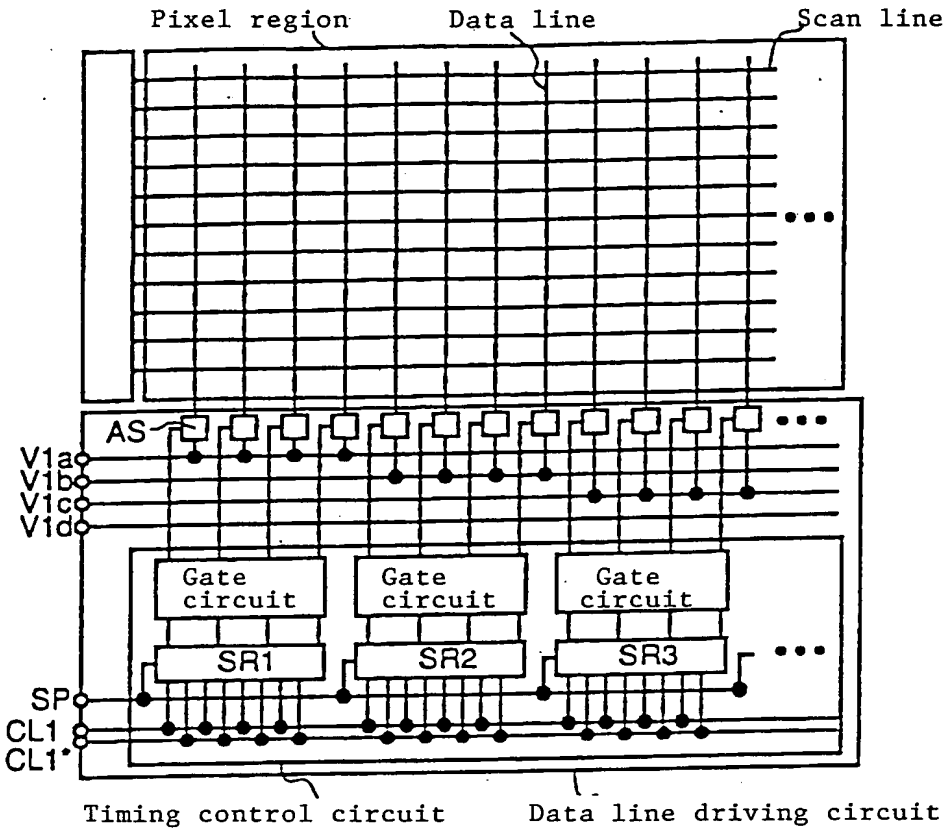

Pixel region
Data line
Scan line
AS
V1a
V1b
V1c
V1d
Gate circuit
Gate circuit
Gate circuit
SR1
SR2
SR3
SP
CL1
CL1*
Timing control circuit
Data line driving circuit

Fig. 8

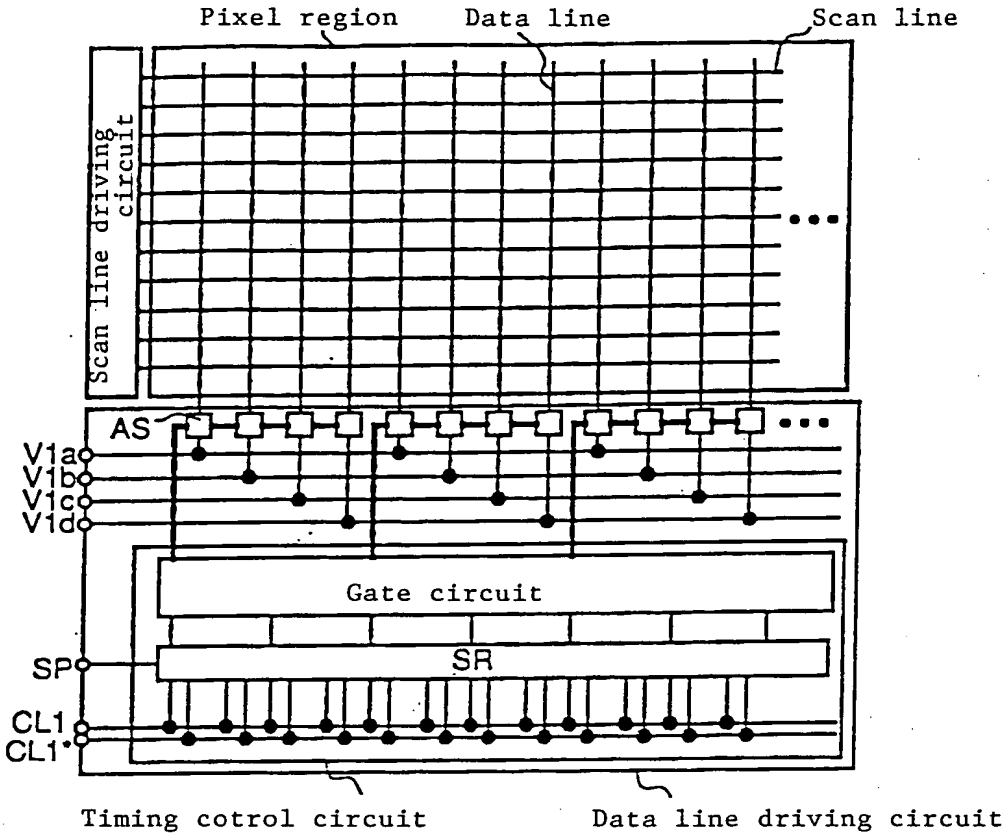

Pixel region
Data line
Scan line
Scan line driving circuit
AS
V1a
V1b
V1c
V1d
Gate circuit
SR
SP
CL1
CL1'
Timing cotrol circuit
Data line driving circuit

Fig. 9

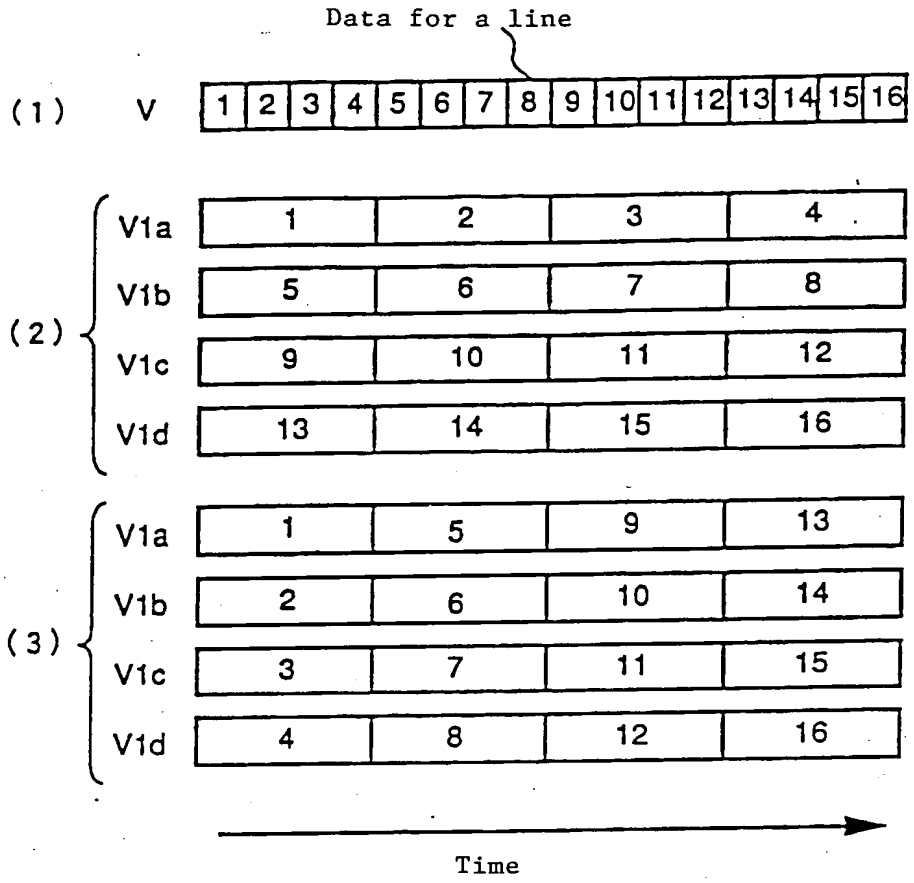

Data for a line
(1) V
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
(2)
V1a 1 2 3 4
V1b 5 6 7 8
V1c 9 10 11 12
V1d 13 14 15 16
(3)
V1a 1 5 9 13
V1b 2 6 10 14
V1c 3 7 11 15
V1d 4 8 12 16
Time

Fig. 10

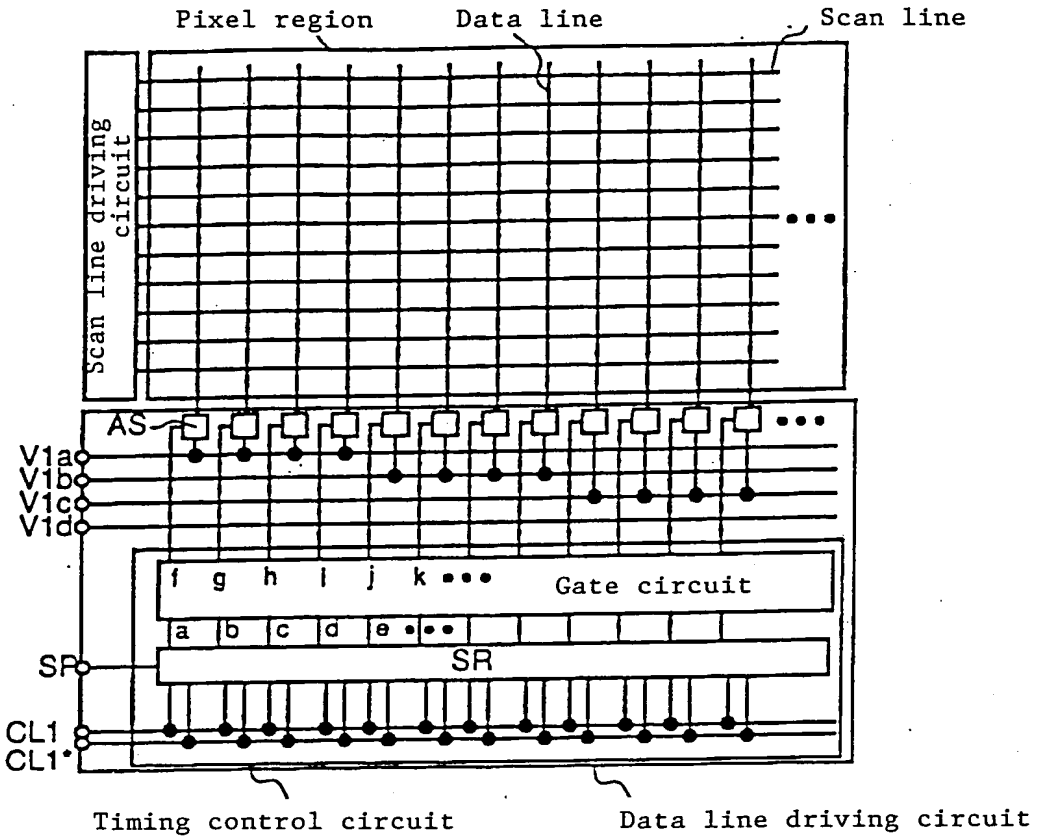

Pixel region
Data line
Scan line
Scan line driving circuit
AS
V1a
V1b
V1c
V1d
f g h i j k
Gate circuit
a b c d e
SR
SP
CL1
CL1'
Timing control circuit
Data line driving circuit

Fig. 11

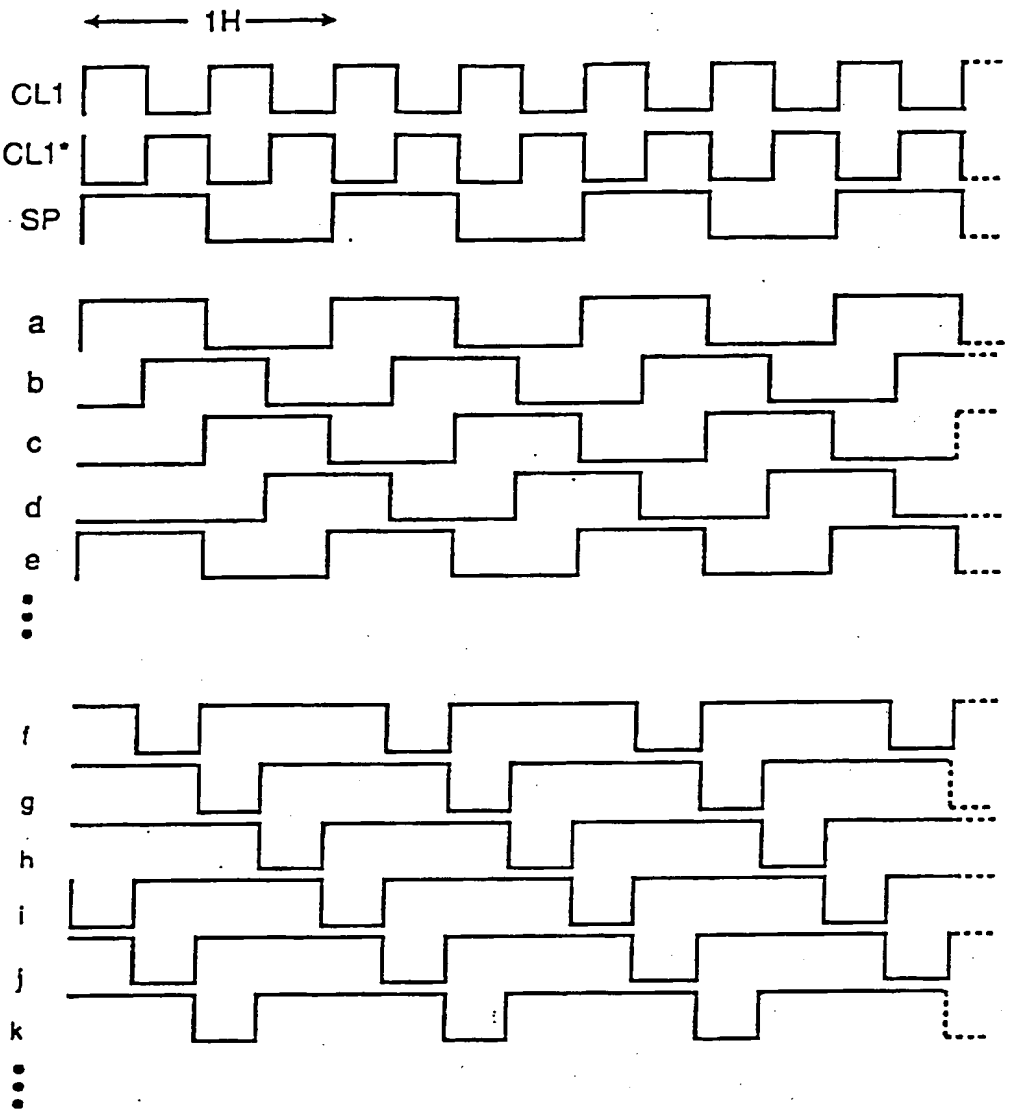


Fig. 12

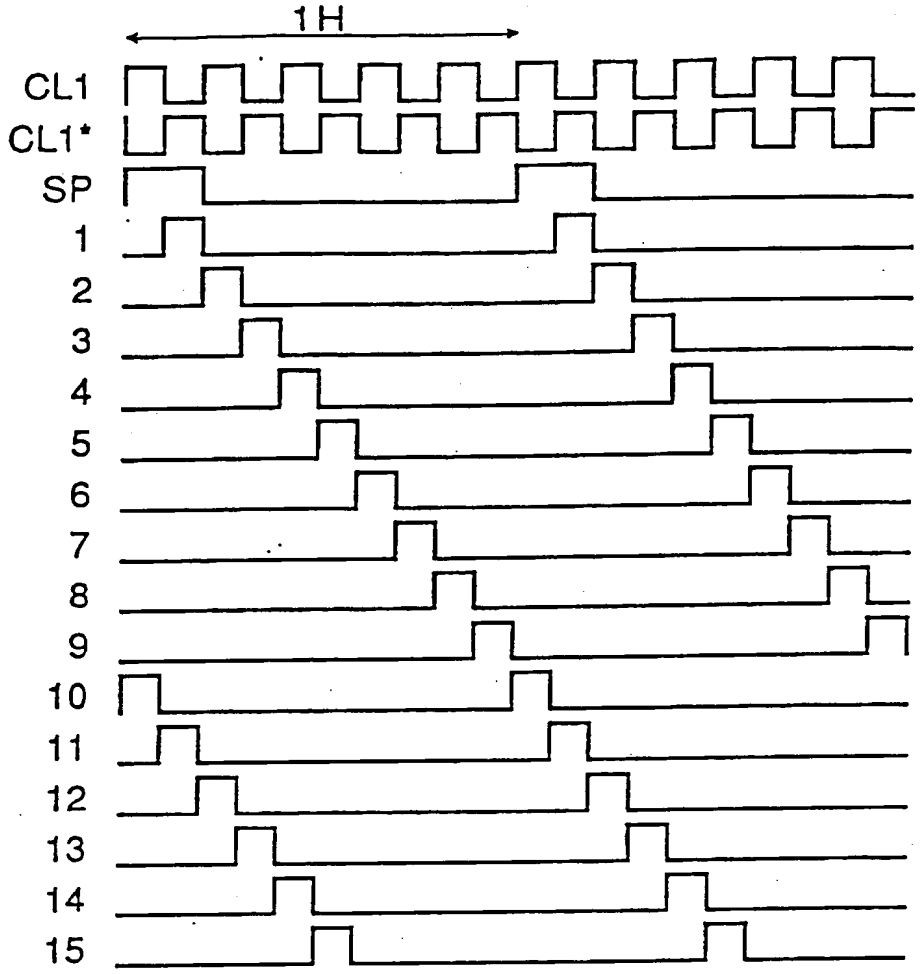


Fig. 13

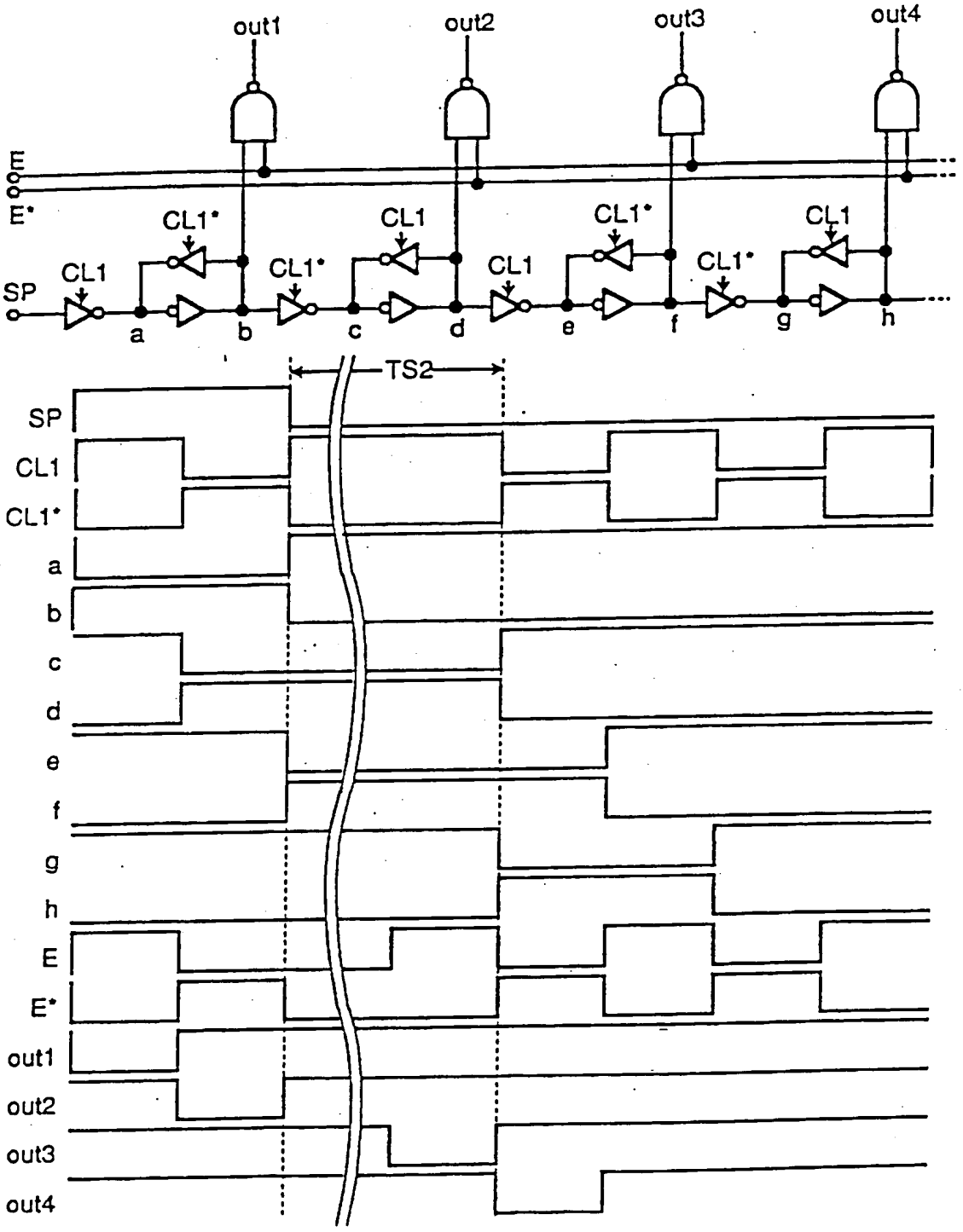

out1
out2
out3
out4
E
E*
CL1*
CL1
SP
a
b
c
d
e
f
g
h
TS2
SP
CL1
CL1*
a
b
c
d
e
f
g
h
E
E*
out1
out2
out3
out4

Fig. 14

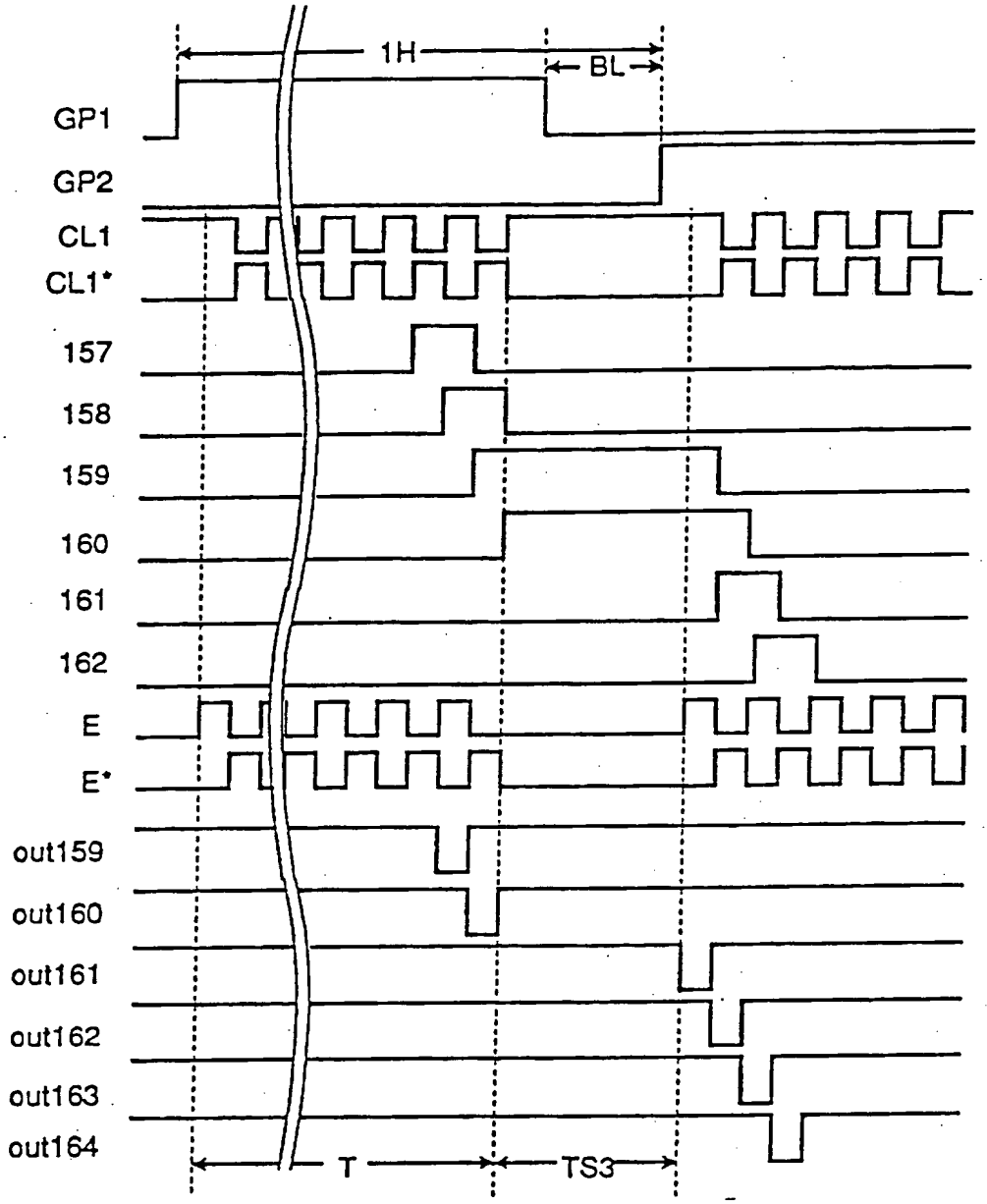

1H
BL
GP1
GP2
CL1
CL1*
157
158
159
160
161
162
E
E*
out159
out160
out161
out162
out163
out164
T
TS3

Fig. 15

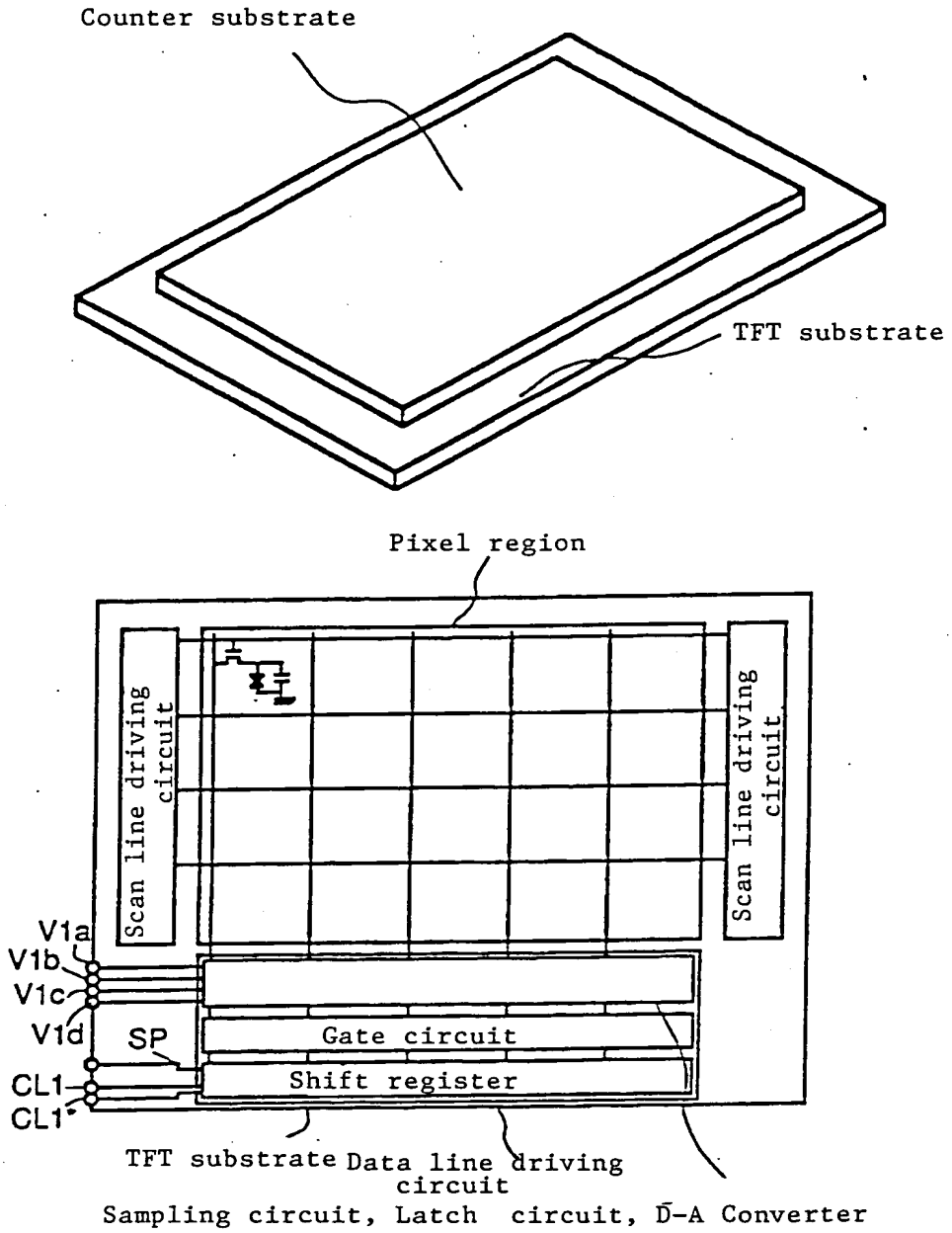
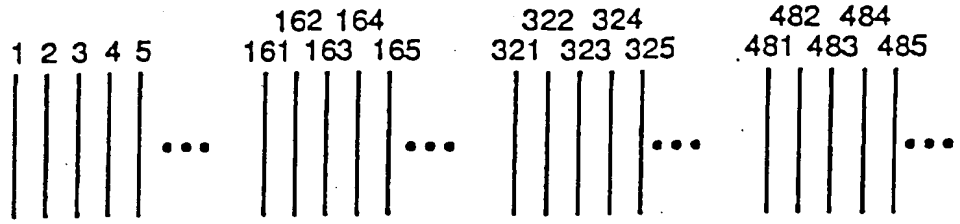

Counter substrate
TFT substrate
Pixel region
Scan line driving circuit
Scan line driving circuit
V1a
V1b
V1c
V1d
SP
CL1
CL1
Gate circuit
Shift register
TFT substrate
Data line driving circuit
Sampling circuit, Latch circuit, D-A Converter

Fig. 16



Time

	1	2	3	4	5	161	162	163	164	165	321	322	323	324	325	481	482	483	484	485
	O					O					O					O				
		O					O					O					O			
			O					O					O					O		
				O					O					O					O	

Output of gate circuit when the video signals are written in

Time

	1	2	3	4	5	161	162	163	164	165	321	322	323	324	325	481	482	483	484	485
	O																			
		O																		
			O																	
				O																

Output of gate circuit at inspection

Fig. 17

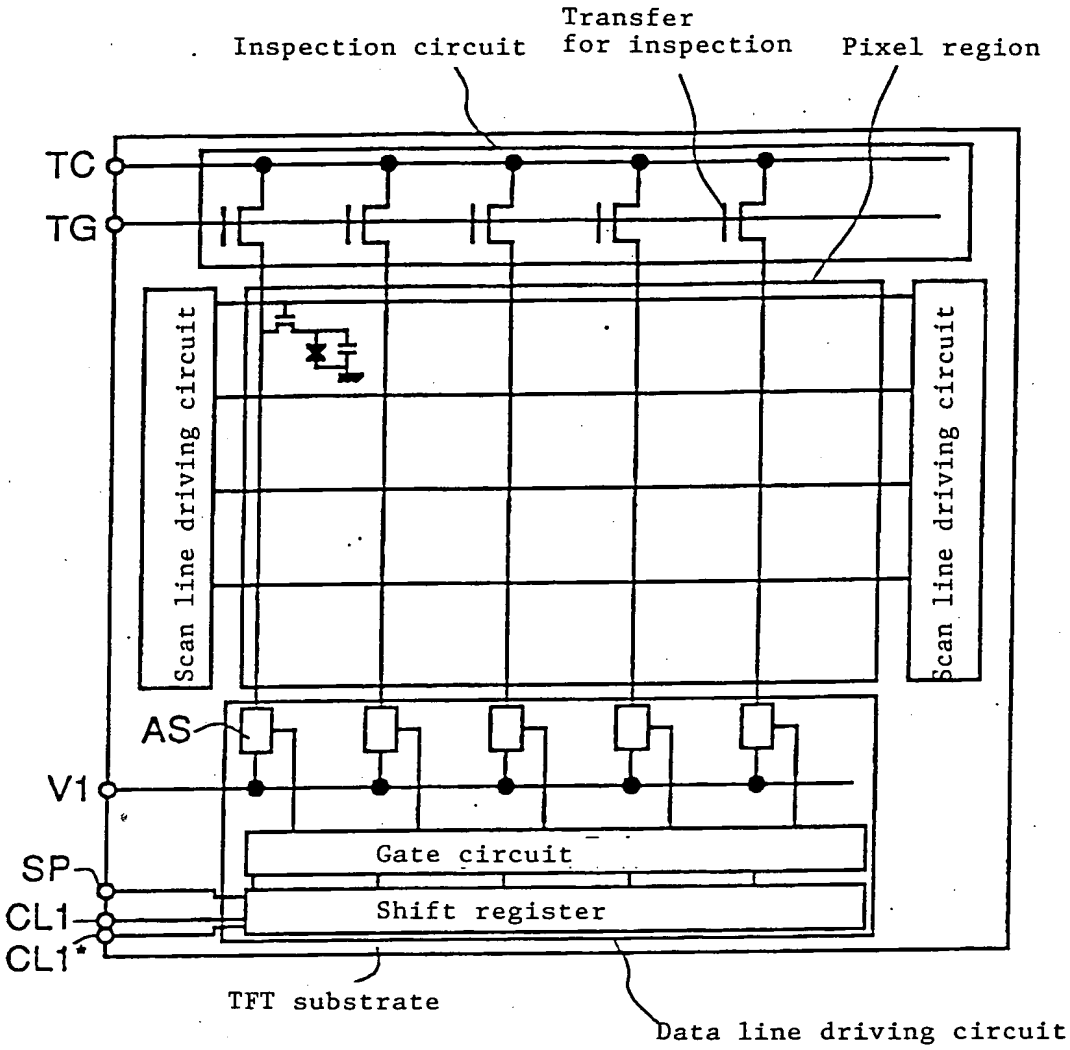

Inspection circuit
Transfer for inspection
Pixel region
TC
TG
Scan line driving circuit
Scan line driving circuit
AS
V1
Gate circuit
SP
Shift register
CL1
CL1*
TFT substrate
Data line driving circuit

Fig. 18

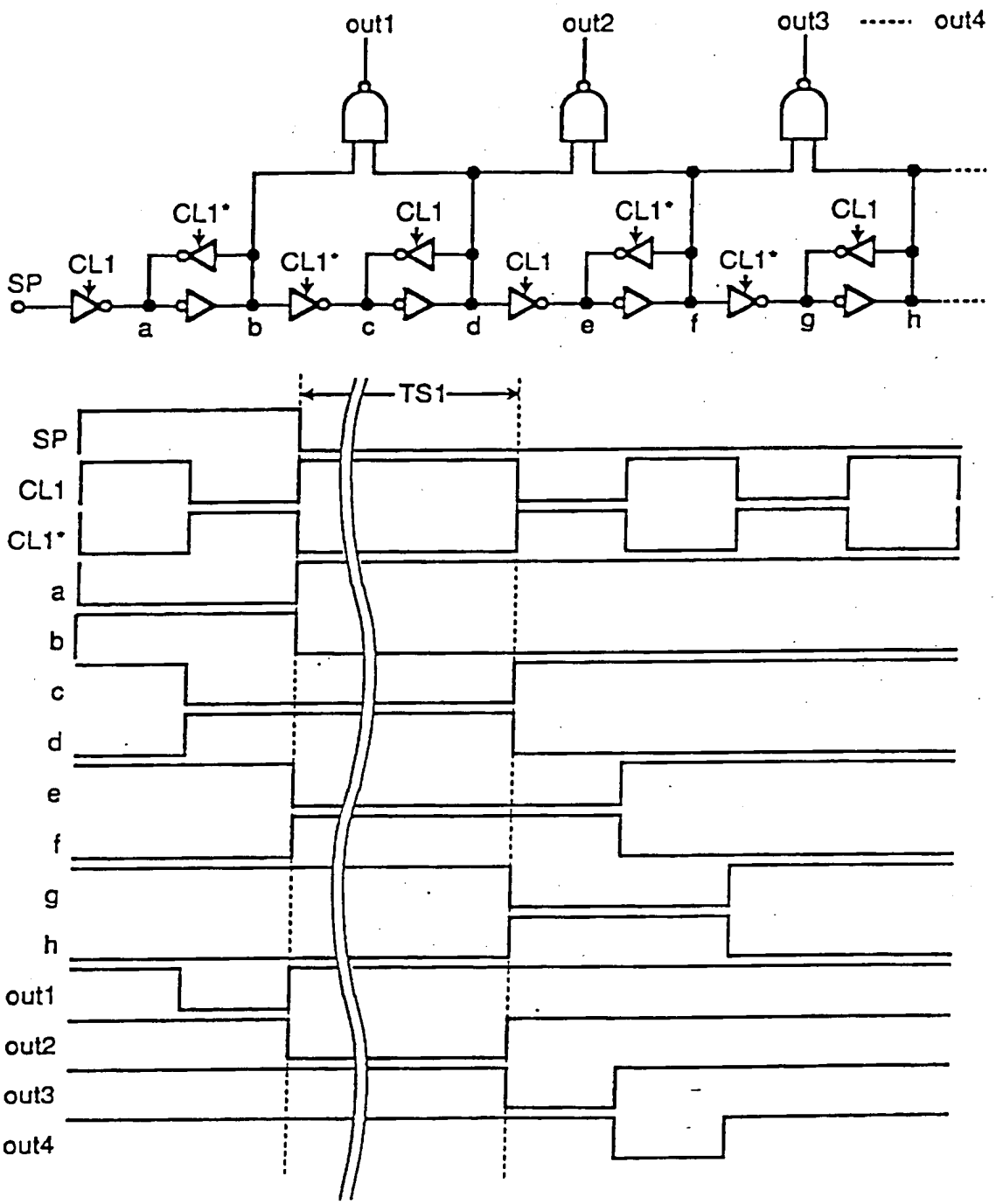


Fig. 19

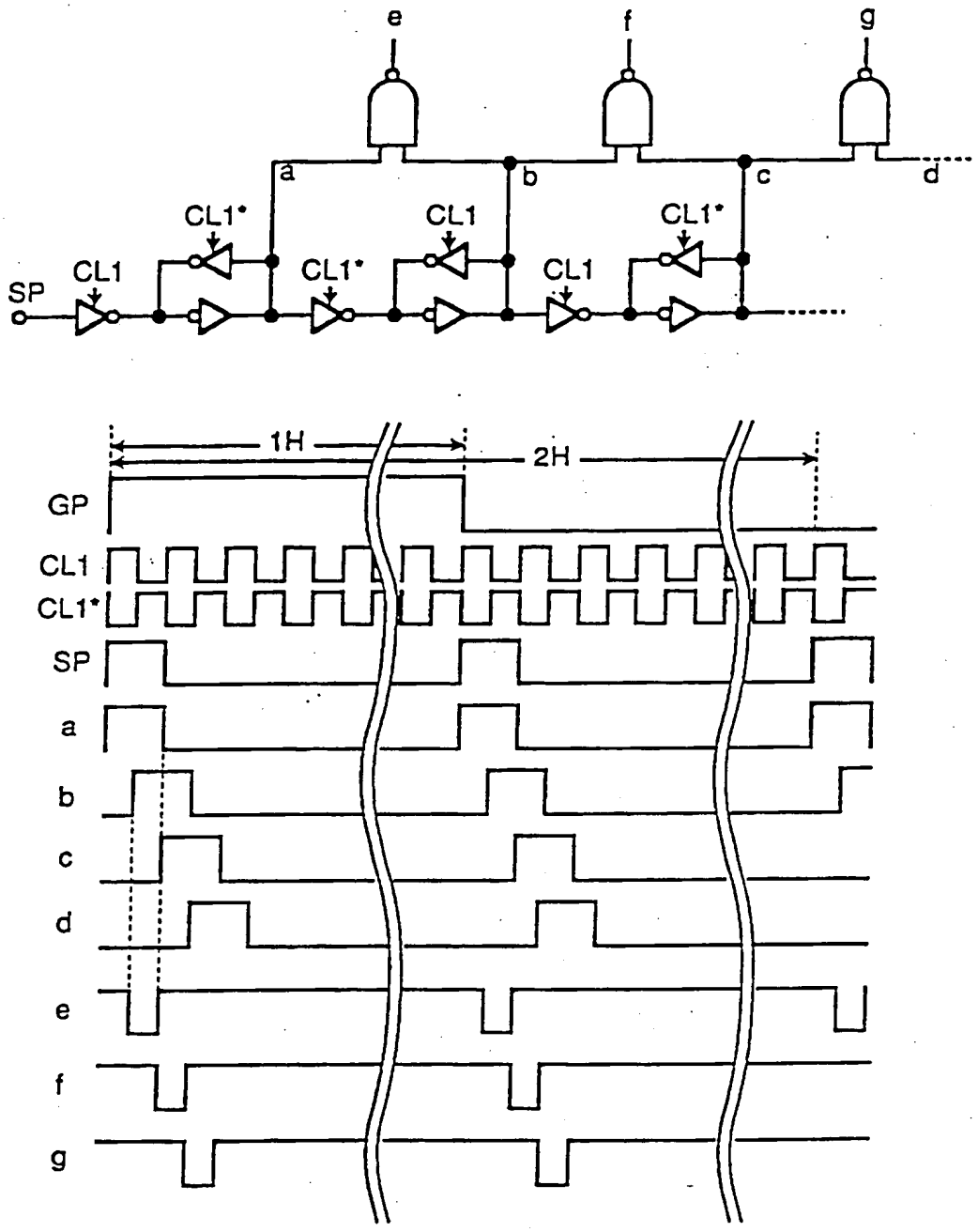
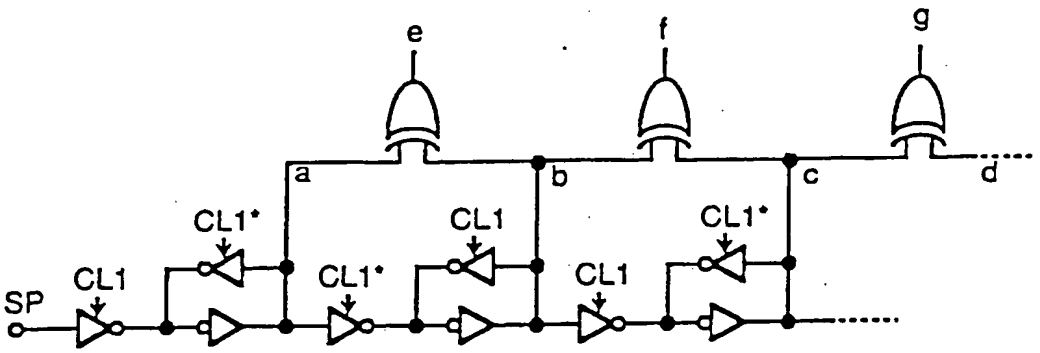


Fig. 20



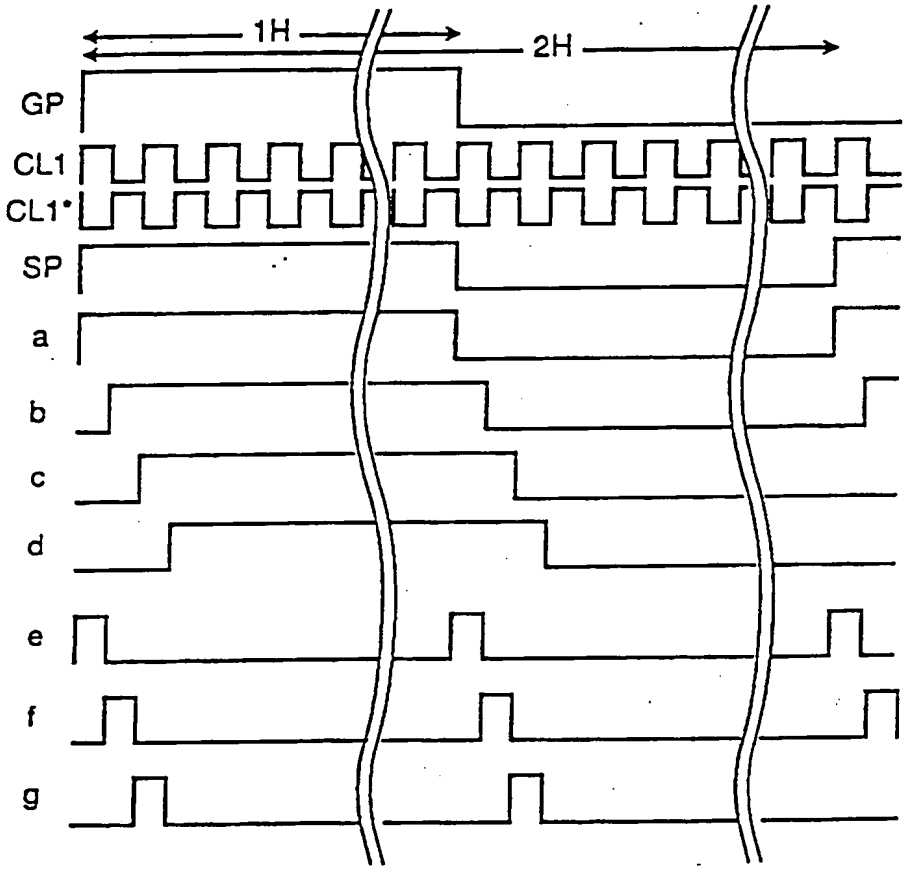
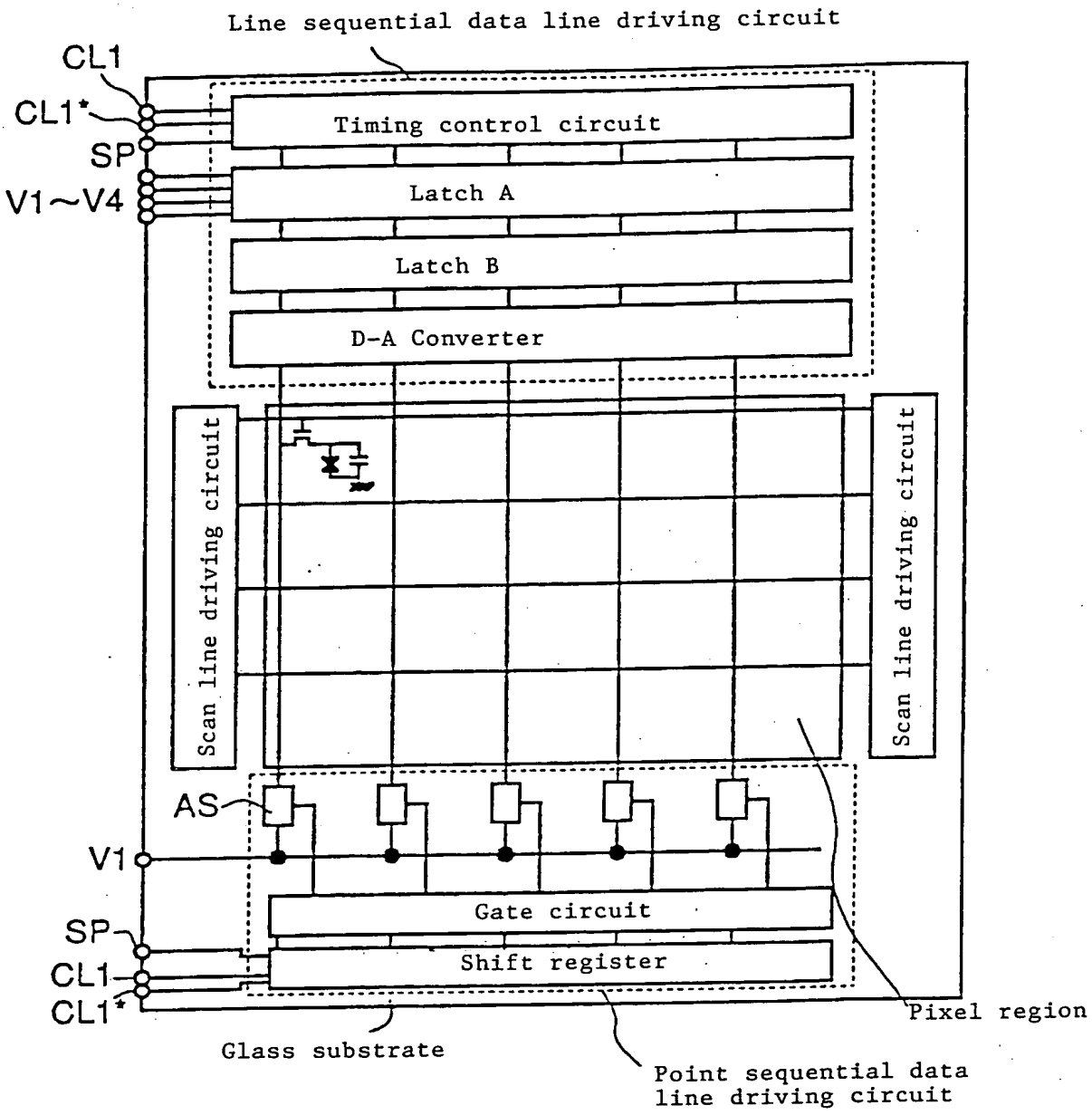


Fig. 21


Line sequential data line driving circuit
CL1
CL1*
SP
V1~V4
Timing control circuit
Latch A
Latch B
D-A Converter
Scan line driving circuit
Scan line driving circuit
AS
V1
Gate circuit
SP
Shift register
CL1
CL1*
Pixel region
Glass substrate
Point sequential data line driving circuit